10

Reset Controls

At reset, certain signal pins are read and the values present, due to pull-ups or pull-downs, are used to initialized bits of particular registers.

Table 10-1   Reset Signal Pins

Name	pin	Description
BaseClassZero	VSAData(0)	1 = force PCI Bass Class Code to be zero
VGAEnable	VSAData(1)	1 = internal VGA subsystem present
VGAFixed	VSAData(2)	1 = enable VGA fixed address decoding
RetryDisable	VSAData(3)	1 = disable PCI Retry using "Disconnect-Without-Data"
ShortReset	VSAData(4)	1 = generate short "AReset" pulse (BusReset + 64 clocks)
AGP1XCapable	VSAData(5)	1 = AGP 1XCapable
SBACapable	VSBData(0)	1 = AGP Sideband Addressing Capable
SubsystemFromRom	VSBData(1)	1 = Load subsystem Vendor ID and SubsystemID from ROM . 0 = leave as reset values
AGP2XCapable	VSAData(6)	1 = AGP 2X Capable
AGP4XCapable	VSAData(7)	1 = AGP 4XCapable - this should never be set on a P3, unless 4X drivers are added
IndirectIOEnable	VSBData(2)	1 = Indirect IO accesses using BaseAddress 3 are enabled
WCEnable	VSBData(3)	0 = Upper half of region Zero is byte-swapped 1= Upper half of region Zero flagged internally as write-combined
PrefetchEnable	VSBData(4)	1 = Base Address registers 1 and 2 marked as prefetchable

A hard configuration pin also exists (Table 10-2).

Table 10-2   Hard Configuration Pin

Name	Pin	Description
PCIClk66	PCIClkSel	0 = up to 33MHz 1 = 66 MHz

Note: Note: During Power-up resets the external frequency reference must be powered at the same time as the Permedia3 or before it, to ensure normal operation.