

# 1

## Functional Overview

### 1.1 Introduction

PERMEDIA 3 is a high performance PCI/AGP graphics processor that balances high quality 3D polygon and textured graphics acceleration, windows acceleration and state-of-the-art MPEG1/MPEG2 playback with a fast integrated SVGA core, integrated RAMDAC and video ports.

PERMEDIA 3 offers significant advances over earlier members of the PERMEDIA product family in both raw performance and functionality. Specific enhancements include:

**Table 1-1 PERMEDIA 3 Enhancement Summary**

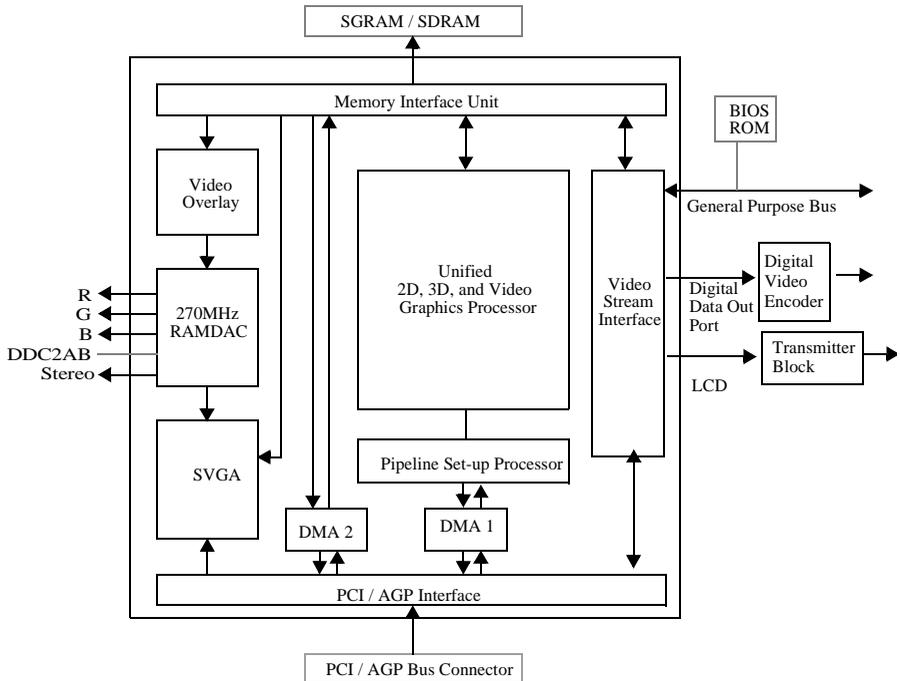
<b>Memory Interface and Core</b>	
Memory bus width (bits)	128
Core clock speed (MHz) - Provisional	125
Max. memory (MB)	32
AGP	2x
RAMDAC speed (MHz)	270
<b>3D</b>	
Max. Z-buffer depth (bits)	32
Non-Linear 16 or 24-bit Z-buffer (Direct3D and OpenGL)	✓
W-Buffer Emulation with Non-Linear Z-buffer (Direct3D)	✓

<b>3D (cont'd)</b>	
Texture read units	2
Texture compositing units	✓
Single-pass dual texturing	✓
Single-pass bump mapping with surface texture	✓
Hardware texture paging	✓
Mip mapping (single pass)	Tri-linear
Destination Alpha	✓
Supports all OpenGL and Direct3D blend modes	✓
Native support for D3D vertex formats	✓
OpenGL	1.2
Fog table	✓
Full hardware edge anti-aliasing	✓
<b>Video/DVD</b>	
Hardware video overlay	✓
Hardware scaling and filtering	✓
MPEG Motion compensation	✓
Memory to DVD accelerator DMA	✓
Flat panel LCD support	✓
<b>Software</b>	
SoftImage Compliant	✓

## 1.2 Functional Blocks

The major functional blocks are shown in Figure 1-1.

**Figure 1-1 Chip Level Block Diagram**



### 1.2.1 AGP/PCI Interface

The PCI interface conforms to the PCI Local Bus standard Revision 2.1. PERMEDIA 3 is a PCI Local Bus Target, a PCI Local Bus Read Master, and a PCI Local Bus Write Master. It is also an AGP read master with support for pipe lined reads and sideband addressing.

The PCI interface has an input FIFO for passing data to the Graphics Core, and an output FIFO for buffering up data to be read from the Graphics Core. The input FIFO is 256 words deep, the output FIFO is 8 words deep. A DMA controller is provided in the PCI interface to allow PERMEDIA 3 to read data directly into the Graphics Core input FIFO or directly out of the output FIFO.

AGP 2X is Intel's high performance, component level interconnect targeted at 3D display applications, which uses a 66MHz PCI specification as an operation baseline and provides three significant performance extension to the PCI specification.

The specification for PERMEDIA 3's AGP implementation is:

- 133 MHz transfer rate (528 Mbytes/s)
- DMA and execute mode support
- Sideband addressing

Implementing these features enables PERMEDIA 3 to achieve 528 Mbytes per second bandwidth from the host for instructions, textures, video data (limited by the host system throughput).

The add-in slot defined for AGP uses a connector body, which is not compatible with the PCI connector, therefore boards designed for use in an AGP slot are not mechanically interchangeable with PCI boards.

## 1.2.2 Unified 2D/3D/Video Integrated Graphics Processor

The graphics core in PERMEDIA 3 accelerates the key operations for 3D and 2D applications. For further information on the functionality of the graphics processor (GP), refer to the *PERMEDIA 3 Programmer's Manual* and chapter 5, Graphics Registers, in this manual.

## 1.2.3 Memory Interface

The local memory is used to store color, depth, stencil, and texture data. For more information on the different data types and usage refer to Chapter 9 - Memory System.

The memory is organized as 1 to 4 blocks (blocks 0-3) of SGRAM or SDRAM. The memory interface is 128 bits wide with control lines for 4 blocks of memories (0-3). Block zero must always be fitted as the SVGA uses this area for local storage. Any other combination of banks may be fitted, but for contiguous memory banks should be added from 1 to 3.

PERMEDIA 3 will make use of special SGRAM features including block fill and write-per-bit masking. SDRAM may be used in place of SGRAM if it is identical to SGRAM except for missing block write and write per bit masks.

### 1.2.4 SVGA and Display Resolutions

The on-chip SVGA unit is register level compatible with standard VGA devices and requires no software emulation. It natively supports all standard VGA modes and certain VESA VBE extended modes.

The standard VESA VBE extended video modes shown below are supported. Those not supportable by the SVGA unit may be supported using the Graphics Processor. Resolution constraints are driver and memory dependant: 1920x1200 is currently supported, but the limits for a 32MByte framebuffer are for example 2048x1200 at 32bit colors, 32bit Z or 2048x1536 at 32bit colors, 16bit Z. At 16bit color, 16bit Z it should be able to display 2400x2400, but this is untested.

**Table 1-2 VESA VBE Graphics Modes**

Mode (hex)	Pixels	Colors	Windowed	Linear	Supportable in SVGA	Supportable in GP
0x100	640x400	256	✓	✓	✓	✓
0x101	640x480	256	✓	✓	✓	✓
0x102	800x600	16	✓	✗	✓	✗
0x103	800x600	256	✓	✓	✗	✓
0x104	1024x768	16	✓	✗	✓	✗
0x105	1024x768	256	✓	✓	✗	✓
0x106	1280x1024	16	✓	✗	✓	✗
0x107	1280x1024	256	✓	✓	✗	✓
0x109	320x200	32K (5:5:5:1)	✓	✓	✗	✓
0x10D	320x200	64K (5:6:5)	✓	✓	✗	✓
0x10F	320x200	16.8M (8:8:8)	✓	✓	✗	✓
0x110	640x480	32K (5:5:5:1)	✓	✓	✗	✓
0x111	640x480	64K (5:6:5)	✓	✓	✗	✓
0x112	640x480	16.8M (8:8:8)	✓	✓	✗	✓
0x113	800x600	32K (5:5:5:1)	✓	✓	✗	✓
0x114	800x600	64K (5:6:5)	✓	✓	✗	✓
0x115	800x600	16.8M (8:8:8)	✓	✓	✗	✓
0x116	1024x768	32K (5:5:5:1)	✓	✓	✗	✓
0x117	1024x768	64K (5:6:5)	✓	✓	✗	✓
0x118	1024x768	16.8M (8:8:8)	✓	✓	✗	✓
0x119	1280x1024	32K (5:5:5:1)	✓	✓	✗	✓
0x11A	1280x1024	64K (5:6:5)	✓	✓	✗	✓
0x11B	1280x1024	16.8M (8:8:8)	✓	✓	✗	✓

The following VESA VBE text modes are supportable in the SVGA:

**Table 1-3 VESA VBE Text Modes**

Mode (hex)	Characters (col/row)
0x108	80x60
0x109	132x25
0x10A	132x43
0x10B	132x50
0x10C	132x60

PERMEDIA 3 allows VESA bankswitching to be done through the bypass to enable additional VESA mode support.

ModeX is also supported.

### 1.2.5 RAMDAC

PERMEDIA 3 incorporates a high performance 270MHz RAMDAC.

Its characteristics include a high resolution 270 MHz 128-bit RAMDAC. It supports screen resolutions up to 1600x1200 with refresh rates of 96Hz or 1920x1080 with refresh rates of 90Hz. It supports packed pixel formats, with color depths of 8, 16, and 32 bits per pixel. It has dot-clock phase locked loops (PLLs) and triple 8-bit D/A converters. The RAMDAC contains a 64x64x2 bit cursor array to support a 2, 4, or 16 color hardware cursor with cursor shapes cache.

### 1.2.6 Video Overlay

The video overlay is used to display incoming video data on screen. the overlay selection is based on a transparent color, the overlay key, which can be any RGB color or alpha value. Optionally, the overlay can be blended with the main image by using a 2-bit blend factor. A filter process supports zooming and shrinking at any rate. It combines four pixels into one by using bilinear filtering to achieve best results. Furthermore the filtered output is optionally converted from YUV to RGB color space format.

## 1.2.7 DMA1..DMA3

### 1.2.7.1 DMA1 Controller - System to Graphics Core and Graphics Core to System

- Autonomous Setup-Fetch parallelism
- No Wait State - maximum transfer rate
- Programable Block Size - large DMA buffers
- Separate DMA Controllers for Upload and Download which can run concurrently

### 1.2.7.2 DMA2 Controller - System to Memory and Memory to System

- Fast texture image uploads and downloads
- Separate DMA Controllers for Upload and Download which can run concurrently
- DMA controller supports scatter/gather
- Fast software MPEG2 download - fast frame capture

### 1.2.7.3 DMA3 Controller - System Memory to DVD accelerator

- Compressed video to DVD accelerator chip Input FIFO
- Fetch/draw parallelism
- Burst mode - bursts for programmed I/O
- DMA controller supports scatter/gather

## 1.2.8 Video Streaming

PERMEDIA 3 supports digital video output. The 24-bit streamed output is designed to work with common PAL/NTSC encoders or flat panel controllers.

## 1.2.9 ROM support

PERMEDIA 3 supports a Flash ROM. This ROM may store code needed for device-specific initialization and the SVGA BIOS.