9
Memory System

The PERMEDIA memory system is intended for use with Synchronous Dynamic Memories. The memories can be SGRAM or SDRAM devices. The width of the memory interface is 128 bits, but can be configured to 64 bits. Control lines are provided for 4 blocks of memories, these are Select (3 – 0). Four ClockOut and ClockReturn signals are also provided, these are to assist in de-skewing the return data and reducing the load on each clock line. The Clock lines should be wired as illustrated in Figure 9.1. The memory system has one set of primary control signals which are common to all blocks, these are Data, Address, RAS, CAS, WriteEnable (WE), DSF, ClkEnable and Byte enables (DQM). A typical organization is shown below.

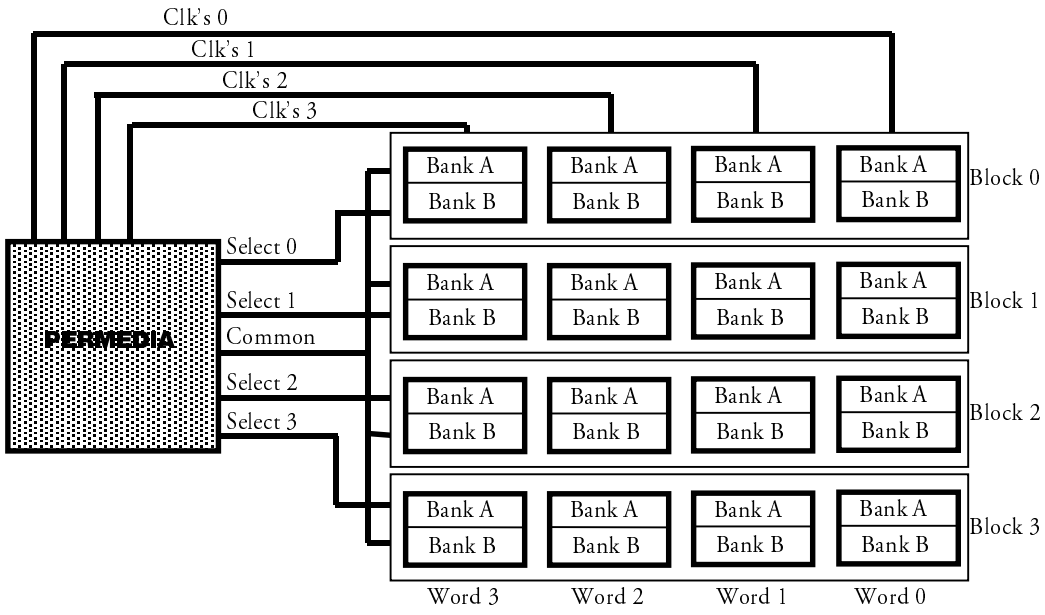


Figure 9.1 Organization of memory devices

The diagram shows a 16-megabyte memory array, constructed from 16, 8-Megabit memories, arranged into 4 blocks. The devices used are 32 bit wide with 2 banks, where each bank has 512 rows and 256 columns.

9.1 System Parameters

The Memory System employs a rich set of registers, which allow for a diverse range of memory configurations. The various timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on memory type, speed grade and the PERMEDIA system clock frequency (MClk). Memory functionally can be enabled depending on the type fitted. Full addressing control is available so that virtually any memory configuration can be fitted.

The following parameters are used to control accesses to the memory. These values fall into three categories

- Addressing
- Functionality and Optimizations
- Timing and Mode

9.1.1 Addressing

9.1.1.1 ColumnAddress

This parameter defines the number of address bits required to generate the column addresses for the memory devices fitted. This parameter is normally quoted in the memory device data sheet.

For example CA7~CA0 therefore the Column Address parameter would be 8

9.1.1.2 RowAddress

This parameter defines the number of address bits required to generate the row addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

For example RA8~RA0 therefore the Row Address parameter would be 9

9.1.1.3 BankAddress

This parameter defines the number of address bits required to generate the bank addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

For example A9(BA) therefore the Bank Address parameter would be 1

9.1.1.4 ChipSelect

This parameter defines the number of address bits needed to select all the blocks of memory devices fitted to the PERMEDIA device.

For 1 Block of memories	Chip Select = 1
For 2 Blocks of memories	Chip Select = 1
For 3 Blocks of memories	Chip Select = 2
For 4 Blocks of memories	Chip Select = 2

9.1.1.5 PageSize

This parameter defines the address range for a memory page of the memory array fitted. The value can be calculated as (column address bits of device – 5). The PageSize parameter modified if either Interleave (0) or Halfwidth (9.1.1.9) are set. PageSize can be calculated as ((column address bits) – 5) + Interleave – Halfwidth.

9.1.1.6 RegionSize

This parameter defines the addressing range for each of the four page-detectors implemented in the memory controller. The minimum region a page-detector can be assigned to is one internal bank, the maximum is all of the memory fitted. There are some memory configurations where not all the page-detectors can be deployed. An example of this is when three blocks of memory devices are used. The value can be calculated as

Where

$$\mathrm{Log2}\left(\frac{\mathrm{TotalMemory}}{\mathrm{BytesperMemWidth} \times \mathrm{RegionsUsed}}\right) - 5$$

TotalMemory = The total size of memory fitted in megabytes

Bytes per Memory Width = 16 (128 / 8)

Regions Used = (if total number of Banks (Blocks fitted x Internal Banks) > 4
then Blocks Fitted
else Total Banks)

As an example the memory configuration in Figure 9-1 is constructed from sixteen 8-megabit devices each with two internal banks

TotalMemory = 16777216 (16-megabytes)

Bytes per Memory Width = 16

Regions Used = (Blocks fitted = 4) x (Internal Banks = 2) = 8
= 8 > 4

$$= 4$$

$$\text{Log2}\left(\frac{16777216}{16\times 4}\right) - 5$$

RegionSize = 13

9.1.1.7 CombineBanks

This flag should be set, when the total number of banks fitted is greater than 4. The total number of banks can be determined by multiplying the number of internal banks of the device by the number of device blocks fitted. In the example shown in Figure 9-1, there are 4 device blocks fitted (Blocks 0 to 3), each device has 2 internal banks (Banks A and B), so the total number of banks is 8, therefore CombineBanks should be set.

9.1.1.8 InterLeave

This flag when set doubles the page size of the memory array. This is accomplished by combining two blocks of memory and operating them as one. Both blocks are PRECHARGED and ACTIVATED together, and any command sequences issued that cross from one block to the other, do so without incurring a page brake. From the example configuration detailed in Figure 9-1, Block 1 would interleave with Block 0, and Block 3 with Block 2. When this flag is set the value loaded into the PageSize parameter (9.1.1.5) should be increased by one. As the Blocks are now operating in pairs the total number of banks fitted is halved. This may have a bearing on the CombineBanks flag (9.1.1.7).

9.1.1.9 HalfWidth

This flag should be set only when the memory buffer fitted is 64 bits wide. When set, this flag has an impact on the PageSize register, (section 9.1.1.5).

9.1.2 Controlling larger memory devices

Permedia3 can drive 64MBx32bit memory devices as follows:

- Tie the CS of the memories Low
- Wire chip Address lines A10 to A0 to memory address lines A10 to A0,
- Wire chip Address line A11 to memory BA0
- Wire chip BankSelect0 to memory BA1

LocalMemCaps register configuration:

Load the register with the value 0x30E311B8. This sets the following parameters:

- Cas address bits 8
- Ras address bits 11
- Bank address bits 1
- ChipSelect bits 1
- Region Size 14

This tactic 'tricks' the Memory Controller into operating as if 2 blocks of twin bank devices are fitted. This approach is reliable and used on a number of **3D***Labs* board products.

9.1.3 Functionality and Optimizations

9.1.3.1 NoPrechargeOpt

This flag when set will disable the back to back READ - PRECHARGE optimization, inserting clocks to the value of the CAS Latency between the commands. If the memory devices fitted are capable of executing a READ command directly followed by a PRECHARGE command, this flag should be left clear for optimal performance. The bit setting cannot be read back directly and should be set or reset when in doubt.

9.1.3.2 SpecialModeOpt

This flag when set enables the memory controller to issue a Special Mode Register Set (SMRS) command, without regard to the current state of the internal banks of the SGRAM. Some memory devices require all internal banks to be in the same state before an SMRS command is issued. For these devices, ensure that the flag is cleared. The memory controller will issue a PRECHARGE command to the devices to ensure all internal banks are in the IDLE mode before issuing the SMRS command. If the memory devices fitted are capable of this function, optimally this flag should be set.

9.1.3.3 TwoColorBlockFill

This flag when set allows the memory controller to utilize the 2 internal Color Registers that some SGRAM devices are equipped with. If the memory devices fitted only have 1 Color Register, this flag should be cleared. When this flag is cleared the memory controller will fully emulate the two color fill operations.

9.1.3.4 NoWriteMask

This flag when set disables the memory controller from using the internal MASK Register of an SGRAM. This flag must be set if SDRAMS are fitted. When this flag is set, the memory controller will emulate the write mask operations. This is only a partial emulation using the byte enables so bit precision is not achieved.

9.1.3.5 NoBlockFill

This flag when set disables the memory controller from issuing a Block Fill command to the memories. This flag must be set if SDRAMS are fitted. When this flag is set the memory controller will fully emulate the block fill operations.

9.1.3.6 NoLookAhead

This flag when set disables the memory controller from issuing command to one bank of memory, whilst another bank is in the process of PRECHARGHING. Nominally for performance, this flag should be left cleared.

9.1.4 Timing and Mode

9.1.4.1 TurnOn (Block to Block Read Delay)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ command to one block of memory devices to a READ of another Block. (Block to Block Read Delay). Two parameters from the memory device data sheet must be used to determine what value TurnOn must be set to. The timing parameter tHZ defines the tri-state time and the parameter tLZ defines the drive time of the device. If tLZ is greater than tHZ, then this parameter can safely be set to zero.

9.1.4.2 TurnOff (Read to Write Turn around)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ and a WRITE command (Read – Write turn around). This parameter is defined in the memory device data sheet, usually as tHZ.

9.1.4.3 RegisterLoad (RL)

This parameter defines the number of MClk cycles that need to be inserted between issuing a SMRS and another command. This parameter is usually detailed in the memory device data sheet as tRSC. If tRSC is quoted including the SMRS cycle, then RegisterLoad should be calculated as tRSC (in MClk cycles) – 1.

9.1.4.4 BlockWrite (BW)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCK WRITE and another command. This parameter is usually detailed in the memory device data sheet as tBWC. If tBWC is quoted including the SMRS cycle, then BlockWrite should be calculated as tBWC (in MClk cycles) – 1.

9.1.4.5 ActivateToCommand (ATC)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a command. This parameter is usually detailed in the memory device data sheet as tRCD. If tRCD is quoted including the ACTIVATE cycle, then ActivateToCommand should be calculated as tRCD (in MClk cycles) – 1.

9.1.4.6 PrechargeToActivate (PTA)

This parameter defines the number of MClk cycles that need to be inserted between issuing a PRECHARGE and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRP. If tRP is quoted including the PRECHARGE cycle, then PreChargeToActivate should be calculated as tRP (in MClk cycles) – 1.

9.1.4.7 BlockWriteToPrecharge (BTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCKWRITE and a PRECHARGE command. This parameter is usually detailed in the memory

device data sheet as tBPL (tBWR). If tBPL is quoted including the BLOCKWRITE cycle, then BlockWriteToPrecharge should be calculated as tBPL (in MClk cycles) – 1.

9.1.4.8 WriteToPrecharge (WTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a WRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRDL (tWR). If tRDL is quoted including the WRITE cycle, then WriteToPrecharge should be calculated as tRDL (in MClk cycles) – 1.

9.1.4.9 ActivateToPrecharge (ATP)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRAS. If tRAS is quoted including the ACTIVATE cycle, then ActivateToPrecharge should be calculated as tRAS (in MClk cycles) – 1.

9.1.4.10 RefreshCycle (RC)

This parameter defines the number of MClk cycles that need to be inserted between issuing and REFRESH and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRC. If tRC is quoted including the REFRESH command cycle, then RefreshCycle should be calculated as tRC (in MClk cycles) – 1.

9.1.4.11 CasLatency (CL)

This parameter determines the CAS latency expected by the memory controller. The CasLatency parameter can be loaded directly with the appropriate value from the memory device data sheet. For example, if a CAS latency of 2 is required then the CasLatency parameter should be set to 2.

9.1.4.12 Mode

This parameter defines the value of the Mode Register loaded into the SGRAM at the end of the boot sequence (see data sheet). Items to note: Burst type should be sequential, burst length should be set to one and CAS latency should be consistent with the CASLatency parameter. For devices that have a Color Register field, this should be consistent with the TwoColorBlockFill flag. All other bits in the Mode field should be set low.

9.1.4.13 RefreshEnable

This flag should be set for Refresh commands to be issued by the memory controller.

9.1.4.14 RefreshCount

This parameter defines the period between AUTO-REFRESH commands being issued to the synchronous memories. The count is in ((MClks/32) + 16) i.e. if RefreshCount = 1, the synchronous memories will be refreshed every 48 MClk cycles. For the required refresh rate, see the synchronous memory data sheet.

9.2 Example Parameter Values

The following device types and values are given as examples and should not be taken as recommendations.

9.2.1 100MHz/Samsung KM4132G271A-10 SGRAM /total SGRAM 12MB

For a PERMEDIA device running with an MClk of 100MHz, fitted with 12, 8Mbit, 2x512x256x32 SGRAMS arranged into 3 Blocks.

Table 9.1 100MHz/Samsung KM4132G271A-10 SGRAM /total SGRAM 12MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1001	9
BankAddress	0001	1 (2 Banks A/B)
ChipSelect	0010	2 (3 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	13 (4 MB)
CombineBanks	1	6 = 3 Blocks x 2Banks
Interleave	0	Optional
HalfWidth	0	Unavailable 128 bit

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	Only 1 Color Register
NoWriteMask	0	Preferred
NoBlockFill	0	Preferred
NoLookAhead	0	Preferred

Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Tshz 7ns
TurnOff (Read to Write)	01	Tshz 7ns
RegisterLoad (RL)	00	New command next Clk
BlockWrite (BW)	01	Tbwc 20ns, 2Clk -1
ActivateToCommand (ATC)	001	Trcd 20ns, 2Clk –1
PrechargeToActivate (PTA)	010	Trp 26ns, 3Clk -1
BlockWriteToPrecharge (BTP)	001	Tbpl 20ns, 2Clk -1
WriteToPrecharge (WTP)	000	Trdl 1Clk -1
ActivateToPrecharge (ATP)	0100	Tras 50ns, 5Clk –1
RefreshCycle (RC)	0111	Trc 80ns 8Clk -1
CasLatency (CL)	011	CasLatency 3
Mode	0000110000	CL3
RefreshEnable	1	
RefreshCount	0110000	64432 Refresh c/s

9.2.2 125MHz[1]/SIEMENS HYB39S16320-7 SGRAM /total SGRAM 16MB

For a PERMEDIA device running with an MClk of 125MHz, fitted with 8, 16Mbit, 2x1024x256x32 SGRAMS arranged into 2 Blocks.

Table 9.2 125MHz/SIEMENS HYB39S16320-7 SGRAM /total SGRAM 16MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1010	10
BankAddress	0001	1 (2 Banks A/B)
ChipSelect	0001	1 (2 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	13 (4 MB)
CombineBanks	0	4 = 2 Blocks x 2Banks
Interleave	0	Optional
HalfWidth	0	Unavailable 128 bit

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	1	Preferred
NoWriteMask	0	Preferred
NoBlockFill	0	Preferred
NoLookAhead	0	Preferred

Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Thz 8ns
TurnOff (Read to Write)	01	Thz 8ns
RegisterLoad (RL)	01	Trsc 2Clk -1
BlockWrite (BW)	01	Tbwc 14ns, 2Clk -1
ActivateToCommand (ATC)	010	Trcd 21ns, 3Clk –1
PrechargeToActivate (PTA)	010	Trp 21ns, 3Clk -1
BlockWriteToPrecharge (BTP)	001	Tbwr 14ns, 2Clk -1
WriteToPrecharge (WTP)	000	Trdl 1Clk -1
ActivateToPrecharge (ATP)	0110	Tras 49ns, 7Clk –1
RefreshCycle (RC)	1001	Trc 70ns 9Clk -1
CasLatency (CL)	010	CasLatency 2
Mode	0001100000	2 Color Reg + CL2
RefreshEnable	1	
RefreshCount	0111100	64566 Refresh c/s

[1] Please note: 125MHz MClk is provisional.

9.2.3 125MHz2/ MICRON MT48LC1M16A1-8A SDRAM /total SDRAM 16MB

For a PERMEDIA device running with an MClk of 125MHz, fitted with 8, 16Mbit, 2x2048x256x16 SDRAMS arranged into 1 Block.

Table 9.3 125MHz/MICRON MT48LC1M16A1-8A SDRAM /total SDRAM 16MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1011	11
BankAddress	0001	1 A/B
ChipSelect	0001	1 (1 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	14 (8 MB)
CombineBanks	0	2 = 1 Block x 2Banks
Interleave	0	Unavailable only 1 block
HalfWidth	0	Unavailable 128 bit

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	Unavailable
NoWriteMask	1	Unavailable
NoBlockFill	1	Unavailable
NoLookAhead	0	Preferred

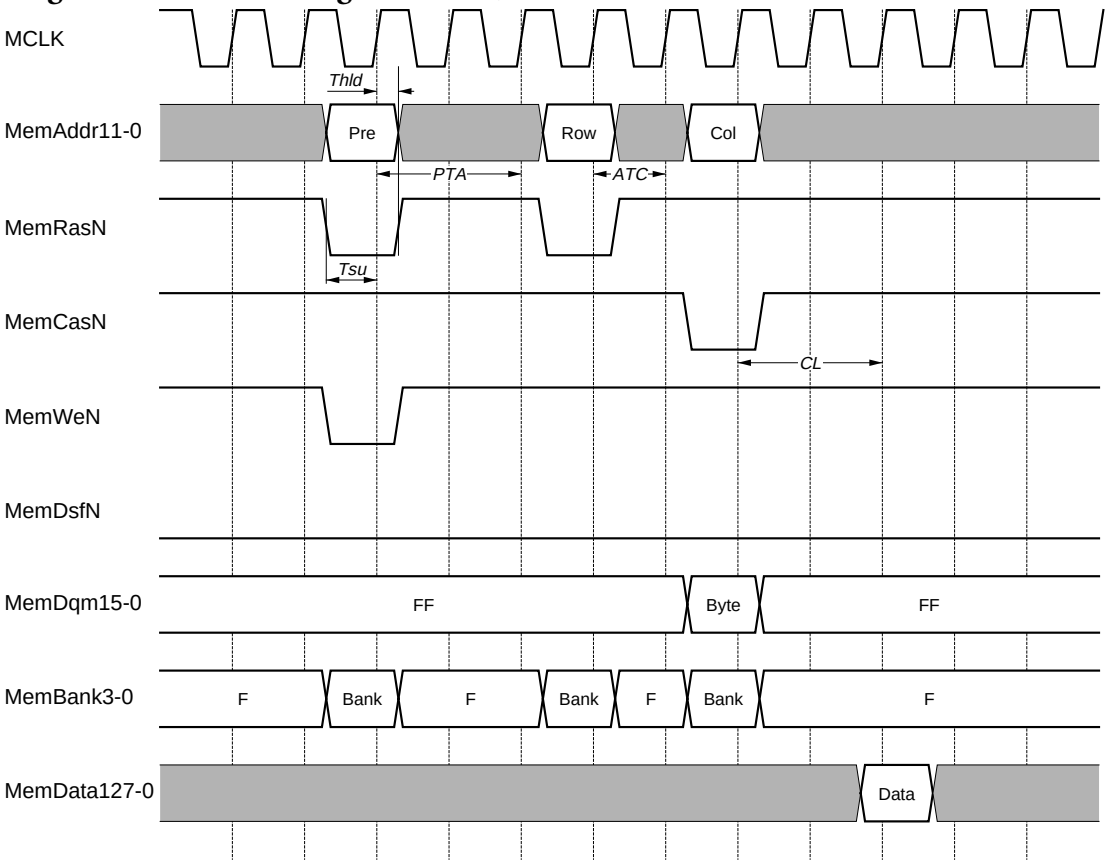
Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Thz 7ns
TurnOff (Read to Write)	01	Thz 7ns
RegisterLoad (RL)	01	Tmrd 2Clk -1
BlockWrite (BW)	00	NA
ActivateToCommand (ATC)	011	Trcd 30ns, 4Clk –1
PrechargeToActivate (PTA)	011	Trp 30ns, 4Clk -1
BlockWriteToPrecharge (BTP)	000	NA
WriteToPrecharge (WTP)	000	Twr 1Clk -1
ActivateToPrecharge (ATP)	0110	Tras 50ns, 7Clk –1
RefreshCycle (RC)	1001	Trc 80ns 10Clk -1
CasLatency (CL)	010	CasLatency 2
Mode	0000100000	CL2
RefreshEnable	1	
RefreshCount	0111100	64566 Refresh c/s

[2] Please note: 125MHz MClk is provisional.

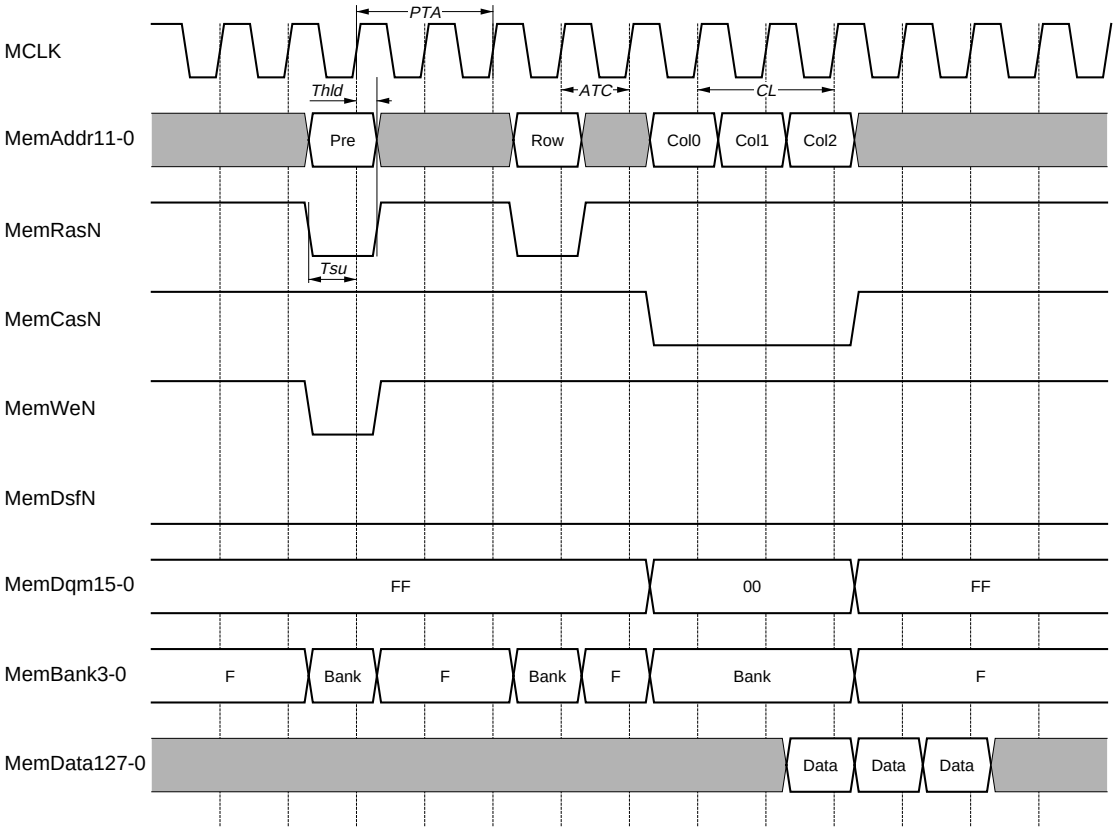
Timing Diagrams

The following timing diagrams show specific operations of the memory controller.

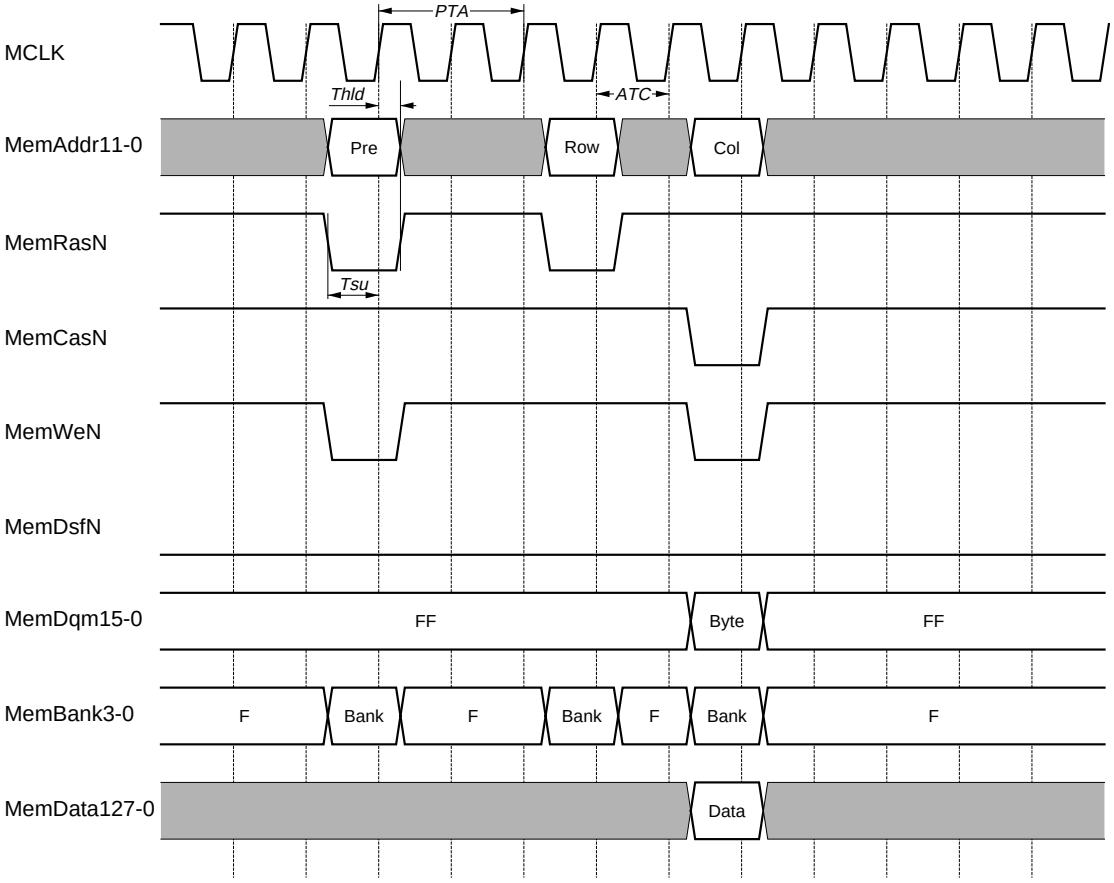
Single Read with Precharge @ CL = 2, PTA = 2 ATC = 1



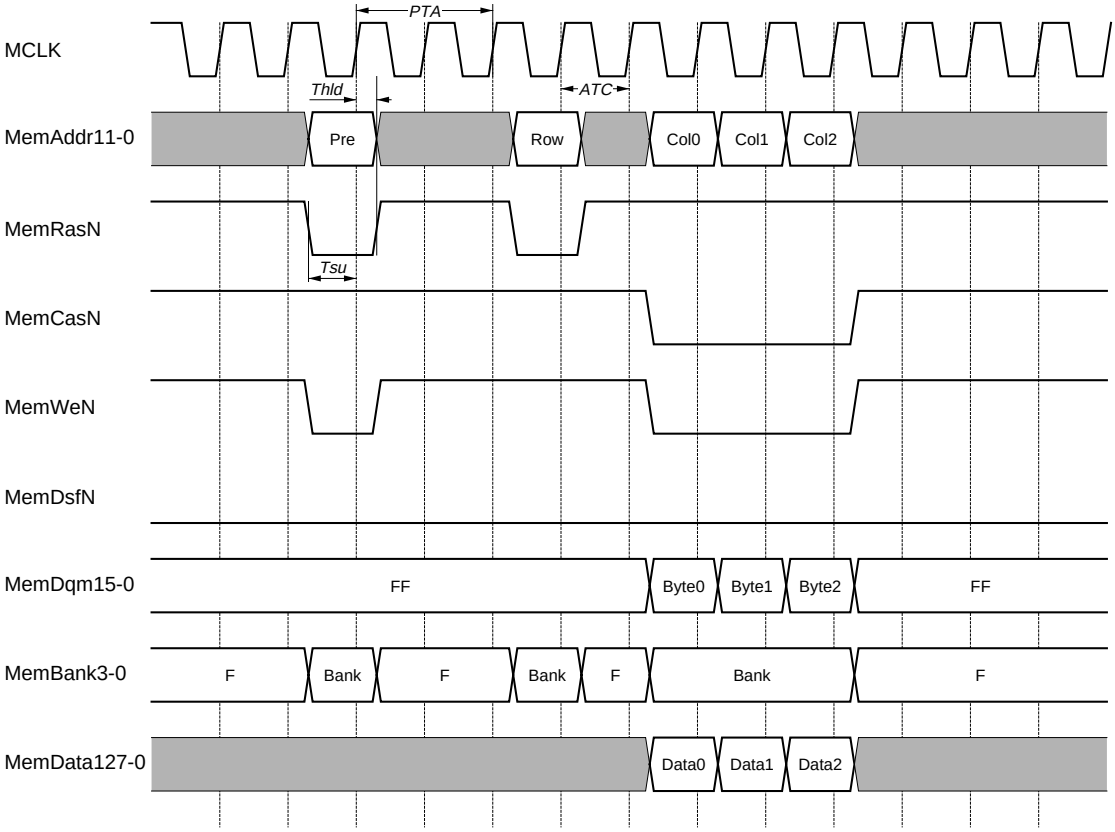
Multiple Reads to Same Bank @ CL = 2, PTA = 2 , ATC = 1



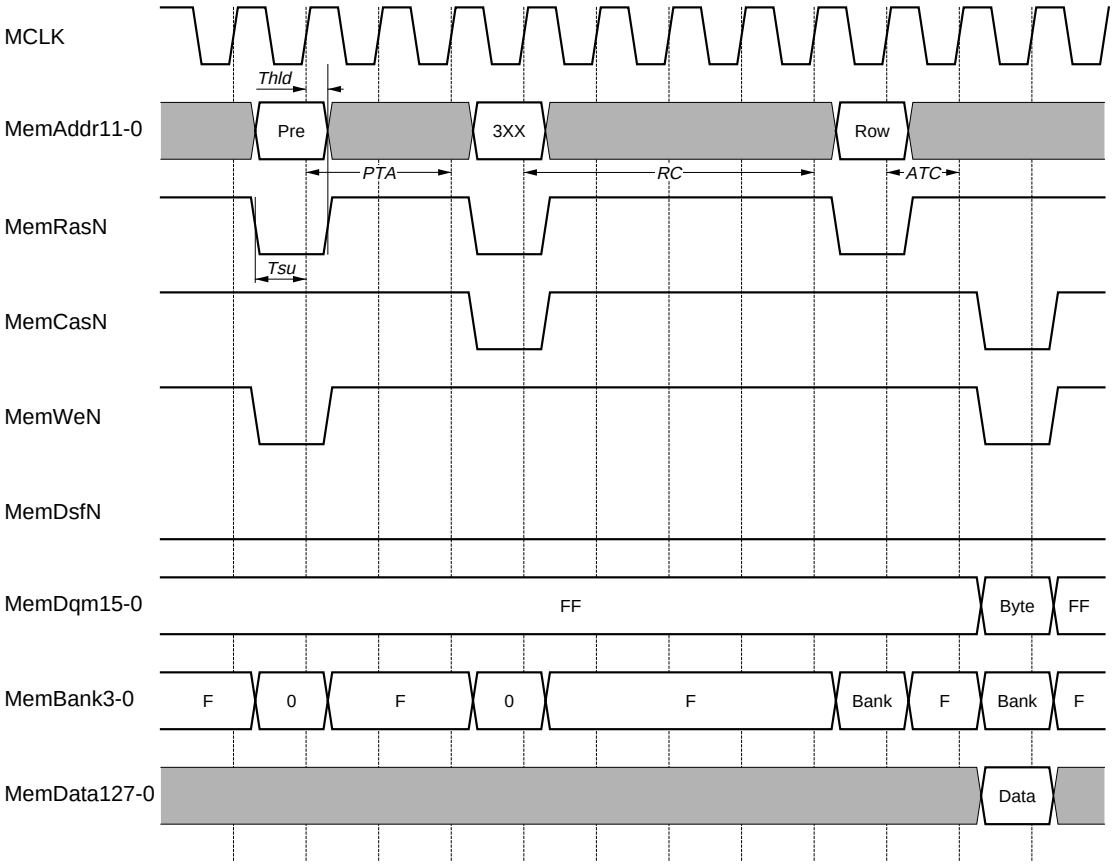
Single Write with Precharge @ PTA = 2, ATC = 1



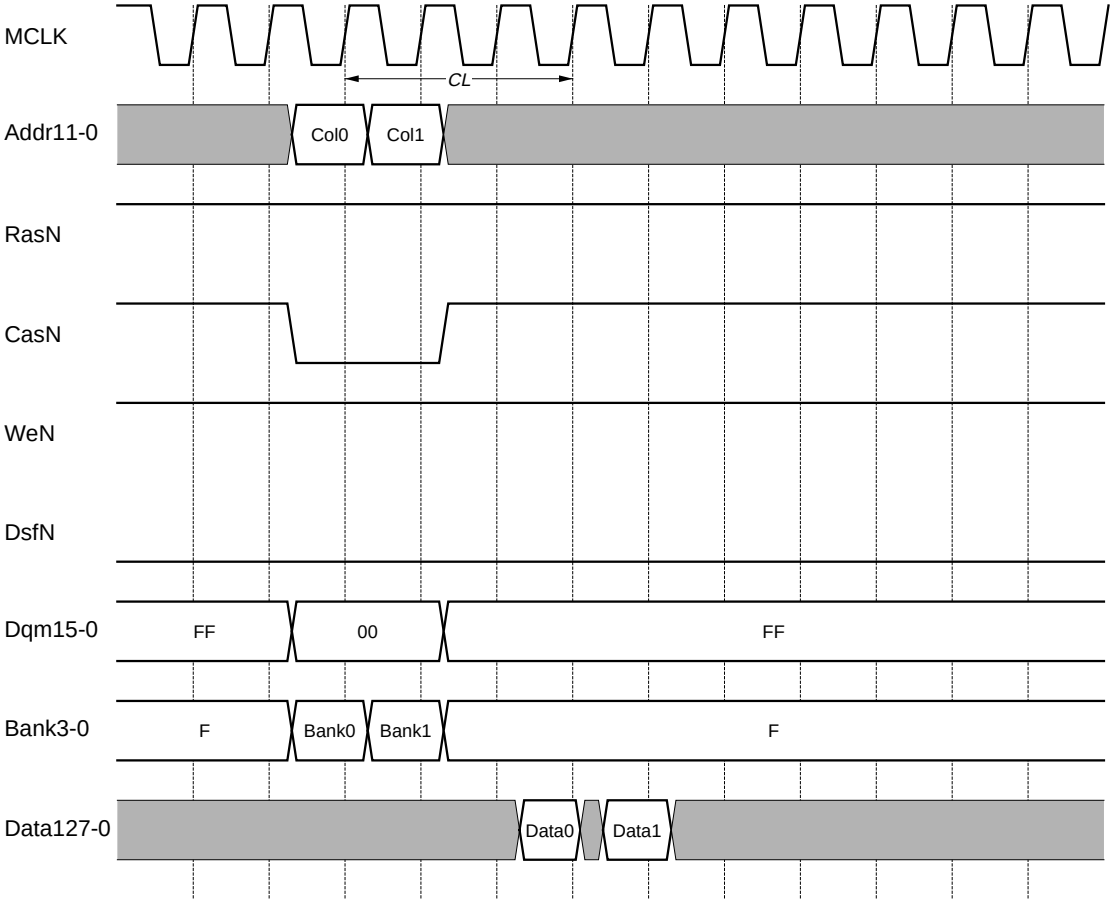
Multiple Writes to Same Bank @ PTA = 2, ATC = 1



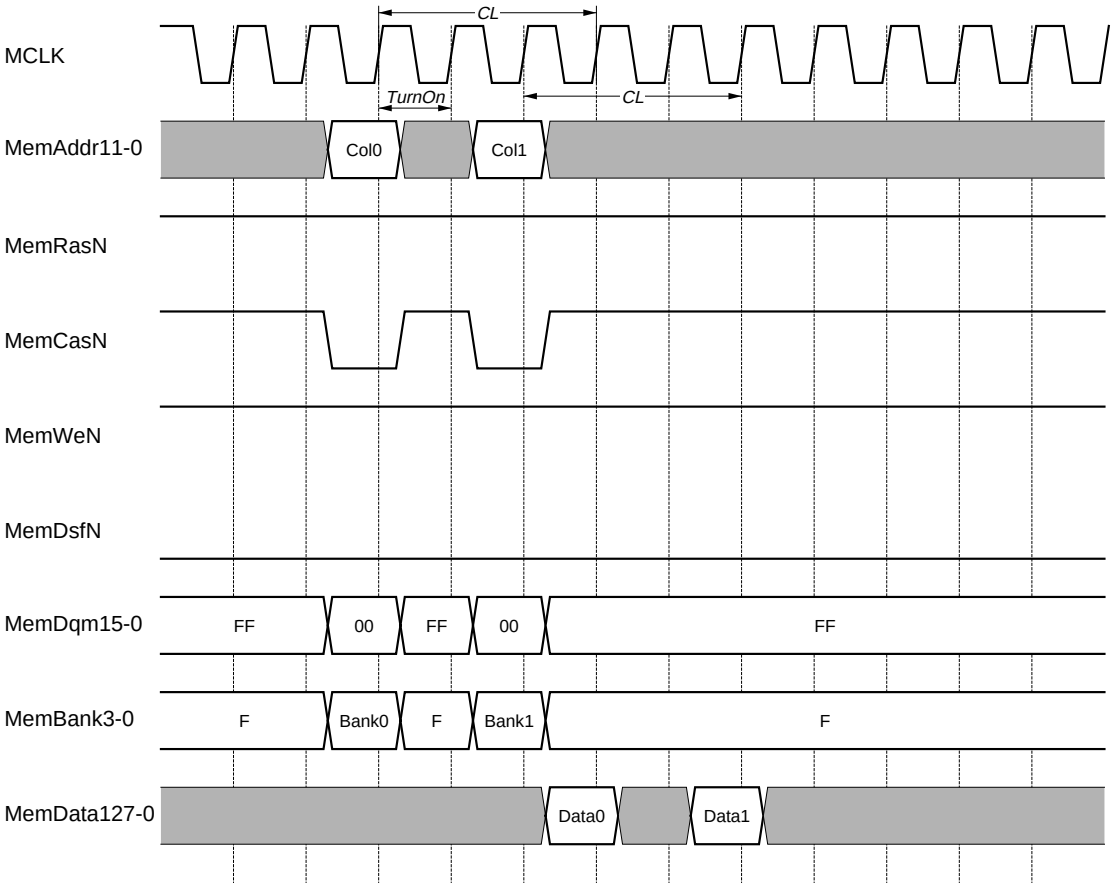
Refresh Followed by Access @ RC = 4, PTA = 2, ATC = 1



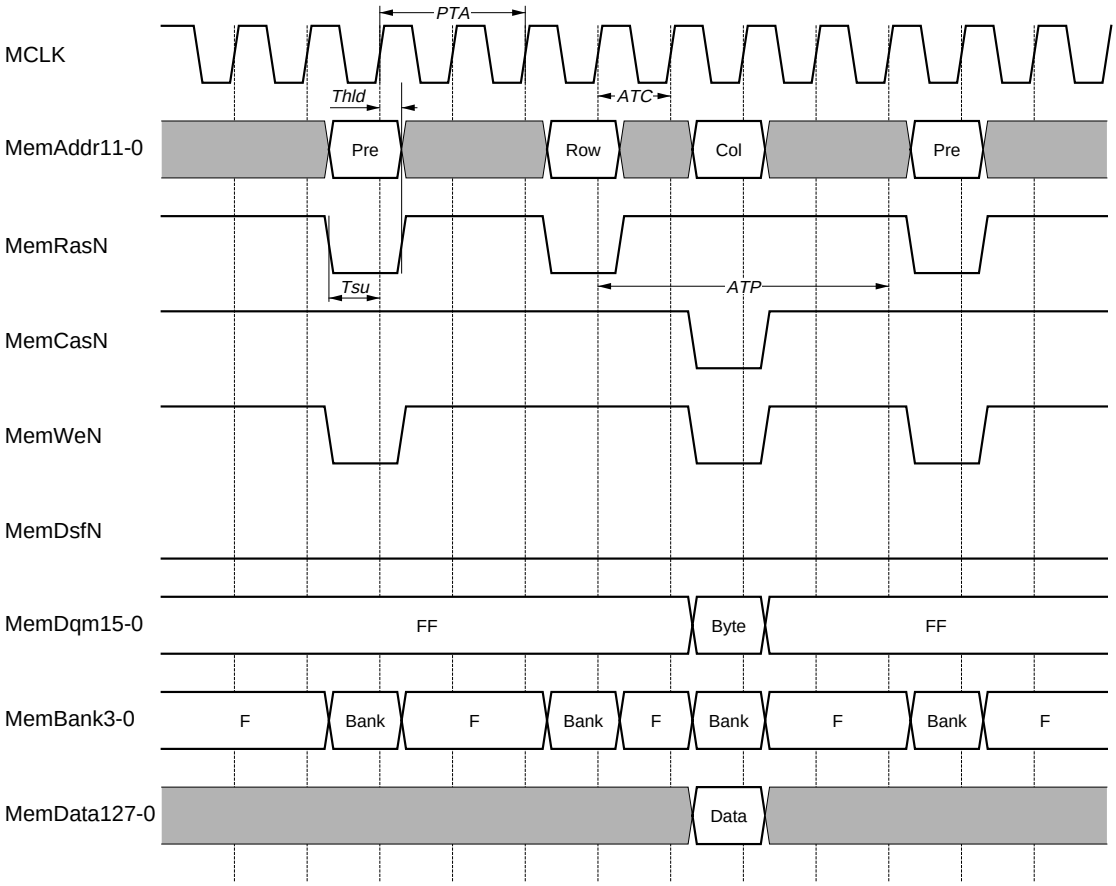
Multiple Reads From Different Banks @ TurnOn = 0, CL = 3



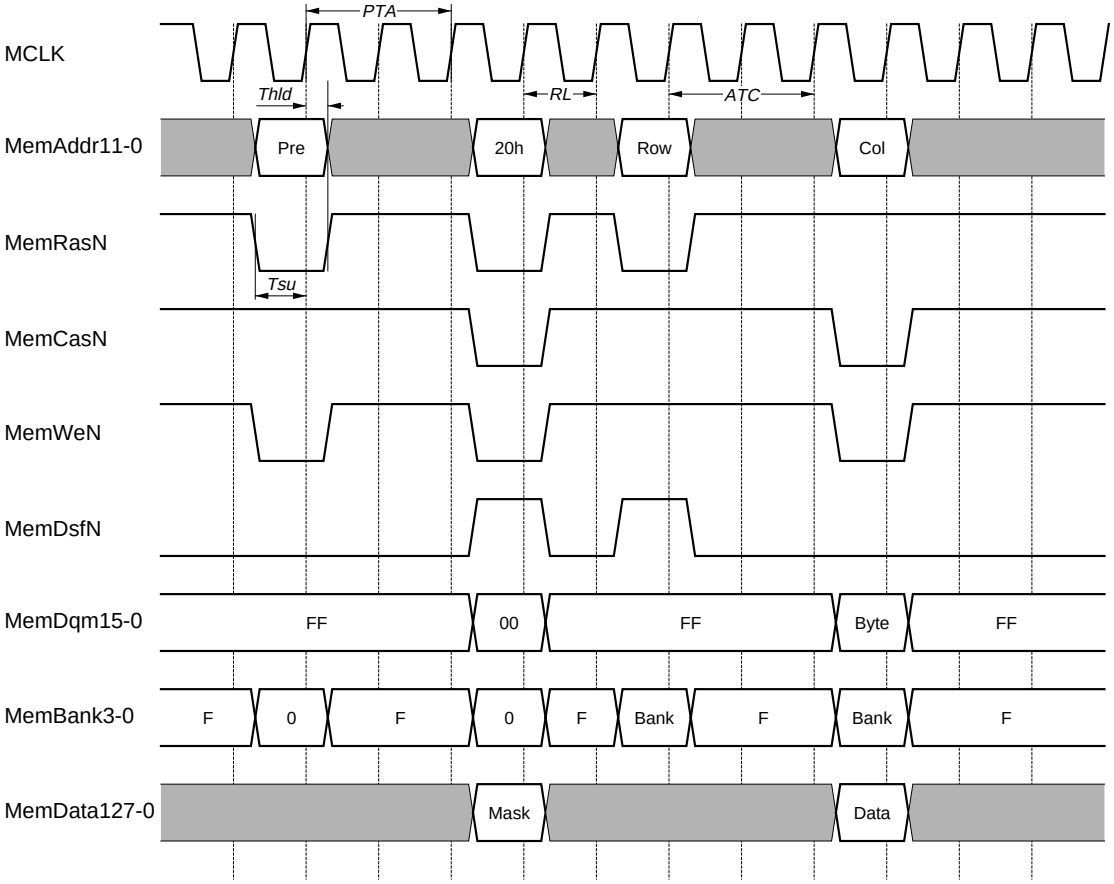
Multiple Reads From Different Banks @ TurnOn = 1, CL = 3



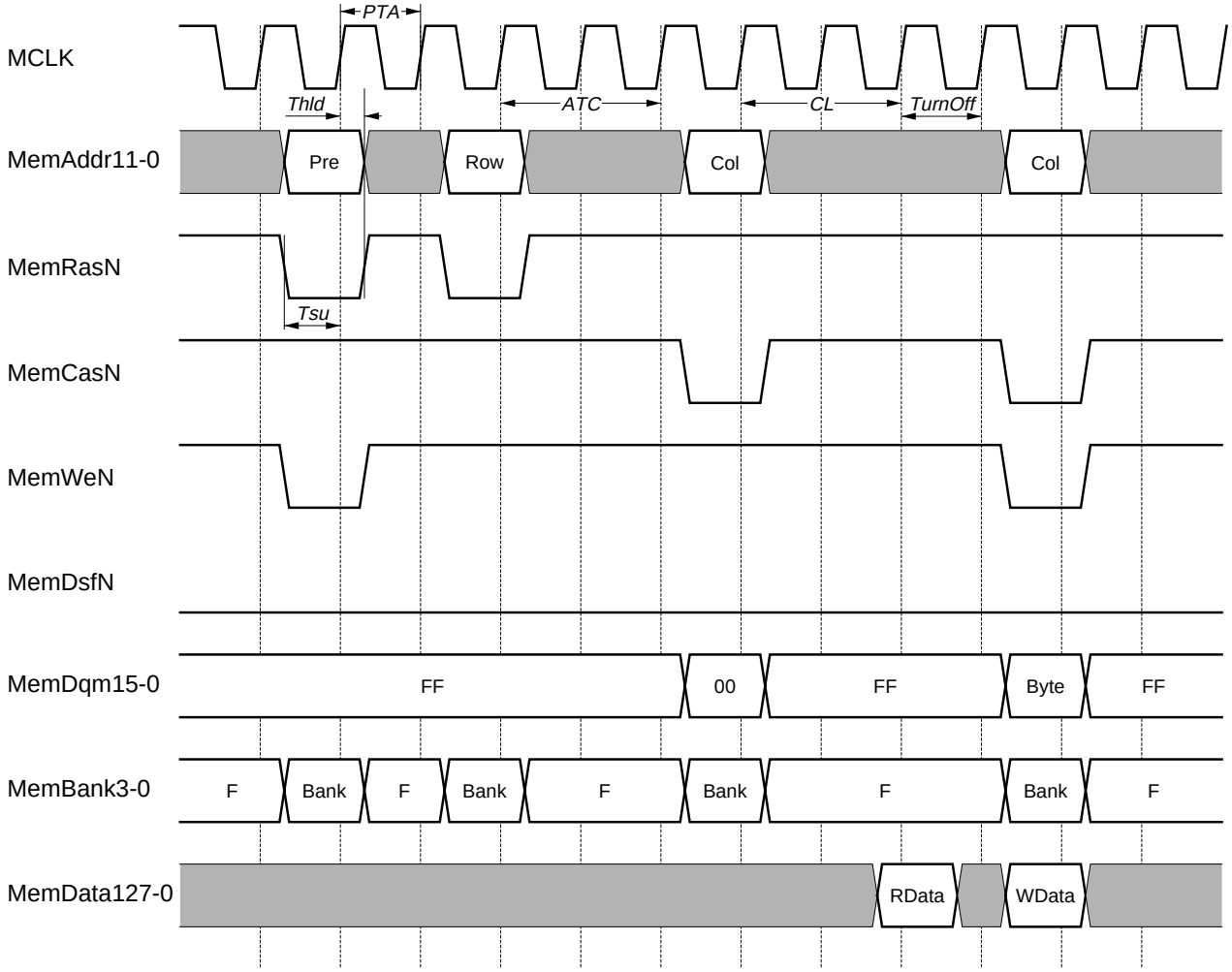
RAS Minimum Access Timing @ ATP = 4



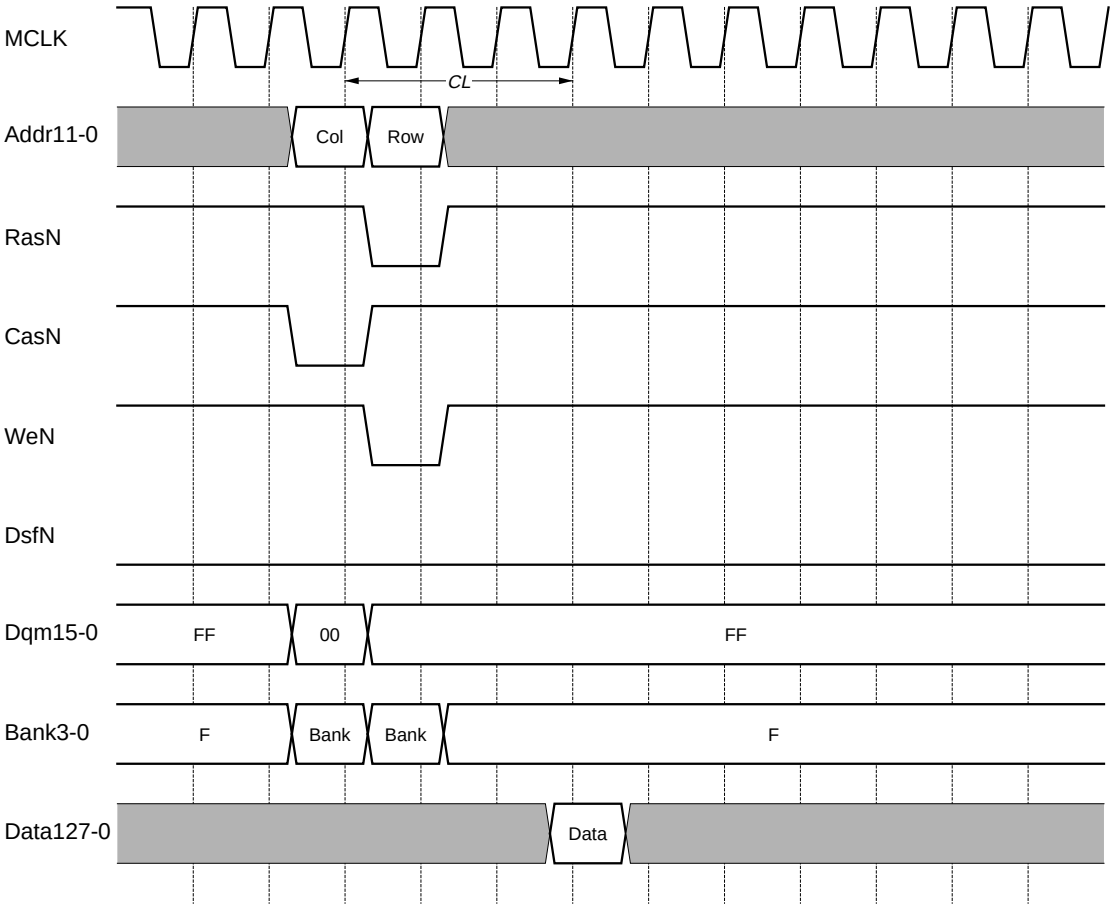
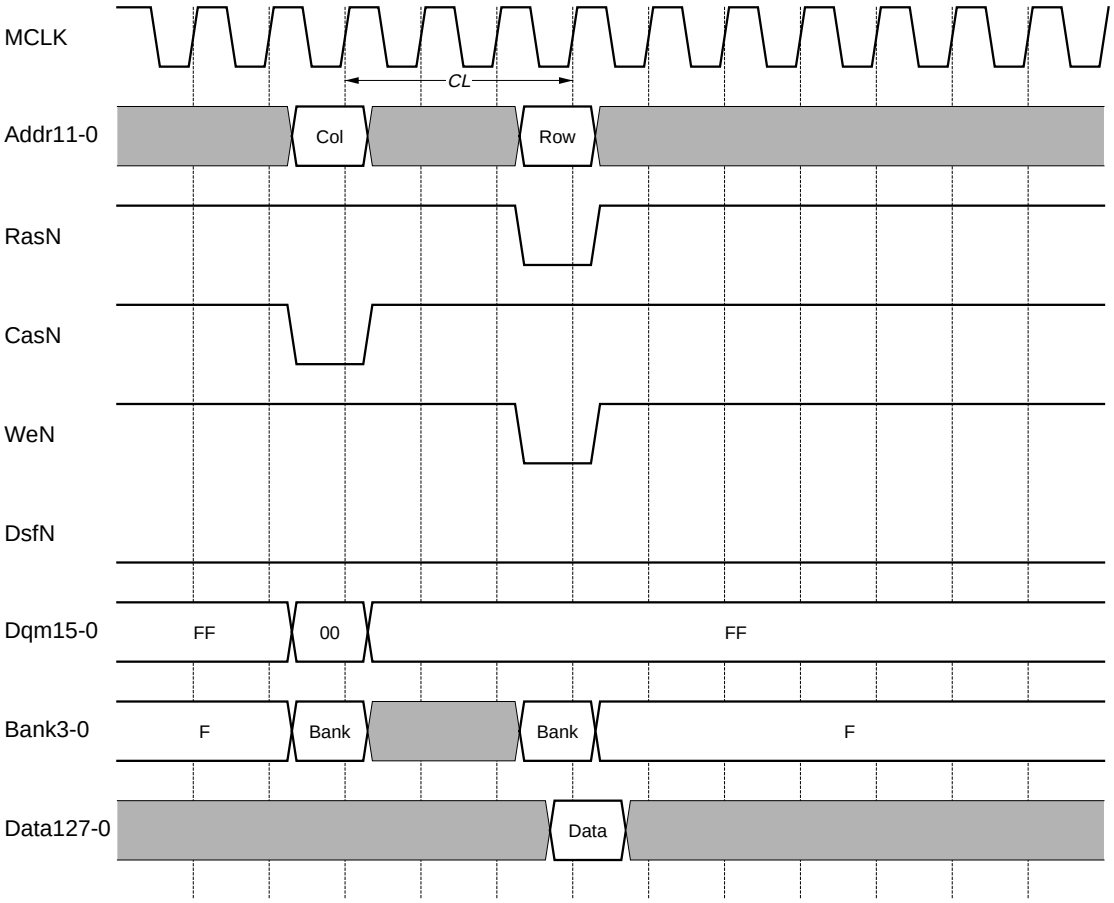
Mask Load Followed by Masked Write @ RL = 1



Read Followed by Write @ TurnOff = 1, CL = 2



Read Followed by PreCharge @ NoPrechargeOpt = 0 , CL = 3



Read Followed by PreCharge @ NoPrechargeOpt = 1, CL = 3