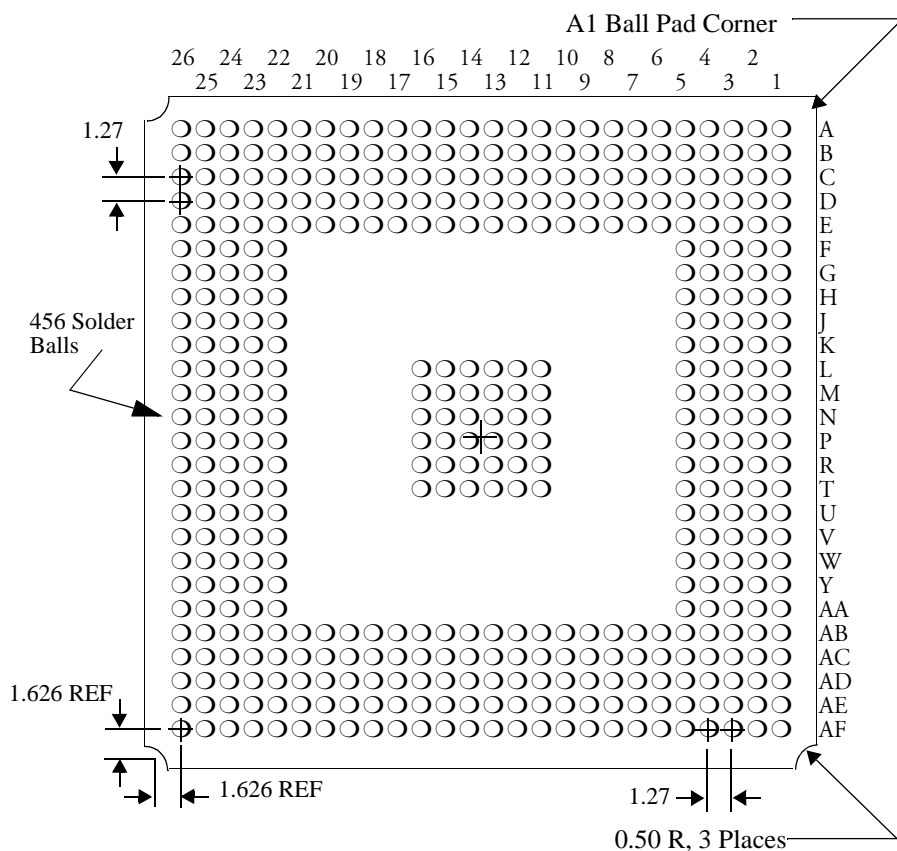# 8

Pin Assignment

Figure 8-1   Package Diagram (Bottom View)

8.1   Pinlist by Number

The table below provides a brief description of each pin. It is organized alphabetically by pin number.

The pin type definitions used are:

- I/O: Input Signal

- GND: Ground

- VSS_3.3: Power at 3.3V

- VSS_2.5: Power at 2.5 Volts

Where AGP pins are unused, the following terminations are recommended:

AGPSBA(7:0)   No connection - output only

AGPPipeN   No connection - output only

AGPADSTB(1:0)   Tie high (input only)

AGPADSTBN(1:0) Tie low (input only)

AGPADSTB   No connection - output only

AGPADSTBN   No connection - output only

AGPADSt(2:0)   Tie high - input only

AGPVREF   As per AGP termination

AGPRbfN   No connection (output only)

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
A1	VCC_2.5	
A2	VCC_2.5	
A3	MDat_124	Memory data line 124
A4	MDat_98	Memory data line 98
A5	MDat_113	Memory data line 113
A6	MDat_112	Memory data line 112
A7	MDat_119	Memory data line 119
A8	MDat_111	Memory data line 111
A9	MDat_104	Memory data line 104
A10	MemClkRet_3	Memory Clock Return 3

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
A11	MDat_90	Memory data line 90
A12	MDat_91	Memory data line 91
A13	MDat_70	Memory data line 70
A14	MDat_82	Memory data line 82
A15	MDat_83	Memory data line 83
A16	MDat_77	Memory data line 77
A17	MDat_76	Memory data line 76
A18	MDat_75	Memory data line 75
A19	MemClkRet_2	Memory Clock Return 2
A20	MDat_60	Memory data line 60
A21	MDat_59	Memory data line 59
A22	MDat_35	Memory data line 35
A23	MDat_36	Memory data line 36
A24	MDat_38	Memory data line 38
A25	VCC_2.5	
A26	VCC_2.5	
B1	VCC_2.5	
B2	VCC_2.5	
B3	MDat_99	Memory data line 99
B4	MDat_97	Memory data line 97
B5	MDat_115	Memory data line 115
B6	MDat_116	Memory data line 116
B7	MDat_108	Memory data line 108
B8	MDat_107	Memory data line 107
B9	MByte_15	Memory byte select 15
B10	MDat_93	Memory data line 93
B11	MDat_89	Memory data line 89
B12	MDat_66	Memory data line 66
B13	MDat_69	Memory data line 69
B14	MDat_81	Memory data line 81

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
B15	MDat_85	Memory data line 85
B16	MDat_78	Memory data line 78
B17	MDat_74	Memory data line 74
B18	MByte_11	Memory byte select 11
B19	MByte_9	Memory byte select 9
B20	MDat_61	Memory data line 61
B21	MDat_58	Memory data line 58
B22	MDat_34	Memory data line 34
B23	MDat_37	Memory data line 37
B24	MDat_39	Memory data line 39
B25	VCC_2.5	
B26	VCC_2.5	
C1	MDat_123	Memory data line 123
C2	MDat_125	Memory data line 125
C3	VCC_2.5	
C4	MDat_96	Memory data line 96
C5	MDat_114	Memory data line 114
C6	MDat_117	Memory data line 117
C7	MDat_109	Memory data line 109
C8	MDat_106	Memory data line 106
C9	MByte_13	Memory byte select 13
C10	MDat_94	Memory data line 94
C11	MDat_88	Memory data line 88
C12	MDat_65	Memory data line 65
C13	MDat_67	Memory data line 67
C14	MDat_80	Memory data line 80
C15	MDat_86	Memory data line 86
C16	MDat_79	Memory data line 79
C17	MDat_73	Memory data line 73
C18	MByte_8	Memory byte select 8

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
C19	MByte_10	Memory byte select 10
C20	MDat_62	Memory data line 62
C21	MDat_57	Memory data line 57
C22	MDat_33	Memory data line 33
C23	MDat_48	Memory data line 48
C24	VCC_2.5	
C25	MDat_49	Memory data line 49
C26	MDat_50	Memory data line 50
D1	MDat_122	Memory data line 122
D2	MDat_100	Memory data line 100
D3	MDat_126	Memory data line 126
D4	VCC_2.5	
D5	MDat_118	Memory data line 118
D6	MDat_110	Memory data line 110
D7	MDat_105	Memory data line 105
D8	MByte_12	Memory byte select 12
D9	MByte_14	Memory byte select 14
D10	MDat_95	Memory data line 95
D11	MDat_92	Memory data line 92
D12	MDat_64	Memory data line 64
D13	MDat_71	Memory data line 71
D14	MDat_68	Memory data line 68
D15	MDat_87	Memory data line 87
D16	MDat_84	Memory data line 84
D17	MDat_72	Memory data line 72
D18	RenderSyncN	Multi-rasterizer i/o sync
D19	MDat_63	Memory data line 63
D20	MDat_56	Memory data line 56
D21	MDat_32	Memory data line 32
D22	VideoExtCtrl	Video External control

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
D23	VCC_2.5	
D24	MDat_51	Memory data line 51
D25	MDat_52	Memory data line 52
D26	MDat_53	Memory data line 53
E1	MDat_121	Memory data line 121
E2	MDat_101	Memory data line 101
E3	MDat_102	Memory data line 102
E4	MDat_127	Memory data line 127
E5	GND	
E6	GND	
E7	VCC_3.3	
E8	VCC_3.3	
E9	GND	
E10	GND	
E11	VCC_3.3	
E12	VCC_3.3	
E13	GND	
E14	GND	
E15	VCC_3.3	
E16	VCC_3.3	
E17	GND	
E18	GND	
E19	VCC_3.3	
E20	VCC_3.3	
E21	GND	
E22	GND	
E23	MDat_47	Memory data line 47
E24	MDat_46	Memory data line 46
E25	MDat_55	Memory data line 55
E26	MDat_54	Memory data line 54

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
F1	MDat_120	Memory data line 120
F2	VSBResetN	Video Stream B Reset Out
F3	MDat_103	Memory data line 103
F4	VSBData_0	VideoStream B data line 0
F5	GND	
F22	GND	
F23	MDat_45	Memory data line 45
F24	MDat_44	Memory data line 44
F25	MDat_43	Memory data line 43
F26	MDat_42	Memory data line 42
G1	VSBData_1	VideoStream B data line 1
G2	VSBData_2	VideoStream B data line 2
G3	VSBData_3	VideoStream B data line 3
G4	VSBData_4	VideoStream B data line 4
G5	VCC_3.3	
G22	VCC_3.3	
G23	MByte_4	Memory byte select 4
G24	MByte_7	Memory byte select 7
G25	MDat_40	Memory data line 40
G26	MDat_41	Memory data line 41
H1	VSBData_5	VideoStream B data line 5
H2	VSBData_6	VideoStream B data line 6
H3	VSBData_7	VideoStream B data line 7
H4	VSBClk	VideoStream B clock
H5	VCC_3.3	
H22	VCC_3.3	
H23	MDat_31	Memory data line 31
H24	MByte_6	Memory byte select 6
H25	MByte_5	Memory byte select 5
H26	MemClkRet_1	Memory Clock Return 1

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
J1	VSGPDataStrob eN	VS GP bus data strobe
J2	VSGPReadWrit eN	VS GP bus read/write signal
J3	VSBClkOut	Video Streams B Clock Out
J4	SPARE	
J5	GND	
J22	GND	
J23	MDat_30	Memory data line 30
J24	MDat_29	Memory data line 29
J25	MDat_28	Memory data line 28
J26	MBank_3	Memory bank select 3
K1	VSCtl_0	VideoStreams Control line 0
K2	VSCtl_1	VideoStreams Control line 1
K3	VSGPChipSelectN	VS GP bus chip select
K4	VSGPDataAckN	VS GP bus data ack
K5	GND	
K22	GND	
K23	MDat_24	Memory data line 24
K24	MDat_25	Memory data line 25
K25	MDat_26	Memory data line 26
K26	MDat_27	Memory data line 27
L1	VSCtl_3	VideoStreams Control line 3
L2	VSCtl_4	VideoStreams Control line 4
L3	VSCtl_5	VideoStreams Control line 5
L4	VSCtl_2	VideoStreams Control line 2
L5	VCC_3.3	
L11	GND	
L12	GND	
L13	GND	
L14	GND	
L15	GND	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
L16	GND	
L22	VCC_3.3	
L23	MDat_3	Memory data line 3
L24	MDat_0	Memory data line 0
L25	MDat_1	Memory data line 1
L26	MDat_2	Memory data line 2
M1	TestSel_0_	Test Mode Select 1
M2	TestSel_2_	Test Mode Select 2
M3	VSCtl_6	VideoStreams Control line 6
M4	VSCtl_7	VideoStreams Control line 7
M5	VCC_3.3	
M11	GND	
M12	GND	
M13	GND	
M14	GND	
M15	GND	
M16	GND	
M22	VCC_3.3	
M23	MDat_7	Memory data line 7
M24	MDat_6	Memory data line 6
M25	MDat_5	Memory data line 5
M26	MDat_4	Memory data line 4
N1	DacAVDD	Analog/video DAC
N2	vidRed	Analog red signal
N3	vidGreen	Analog green signal
N4	VidRightEye	Right signal for stereo
N5	GND	
N11	GND	
N12	GND	
N13	GND	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
N14	GND	
N15	GND	
N16	GND	
N22	GND	
N23	MDat_16	Memory data line 16
N24	MDat_19	Memory data line 19
N25	MDat_18	Memory data line 18
N26	MDat_17	Memory data line 17
P1	VidVRef	Voltage reference
P2	DacComp	Compensation pin
P3	vidBlue	Analog blue signal
P4	vidResRef	Reference resistor
P5	GND	
P11	GND	
P12	GND	
P13	GND	
P14	GND	
P15	GND	
P16	GND	
P22	GND	
P23	MDat_20	Memory data line 20
P24	MDat_23	Memory data line 23
P25	MDat_22	Memory data line 22
P26	MDat_21	Memory data line 21
R1	TestMode	Test Mode control
R2	VidHSync	Horizontal sync
R3	TestSel_1	Test Mode Select 1
R4	DacAGnd	DAC Power/Gnd pin
R5	VCC_3.3	
R11	GND	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
R12	GND	
R13	GND	
R14	GND	
R15	GND	
R16	GND	
R22	VCC_3.3	
R23	MDat_15	Memory data line 15
R24	MDat_14	Memory data line 14
R25	MDat_13	Memory data line 13
R26	MDat_12	Memory data line 12
T1	Xtal1	Crystal i/p 1
T2	VidVsync	Vertical sync
T3	PLLDISABLE	PLL Disable
T4	Xtal2	Crystal i/p 2
T5	VCC_3.3	
T11	GND	
T12	GND	
T13	GND	
T14	GND	
T15	GND	
T16	GND	
T22	VCC_3.3	
T23	MDat_11	Memory data line 11
T24	MDat_8	Memory data line 8
T25	MDat_9	Memory data line 9
T26	MDat_10	Memory data line 10
U1	ROMWeN	ROM Write Enable
U2	ROMSelN	ROM Select signal
U3	VidDDCData	Data line for DDC
U4	VidDDCClk	Clock line for DDC

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
U5	GND	
U22	GND	
U23	MBank_2	Memory bank select 2
U24	MByte_0	Memory byte select 0
U25	MByte_3	Memory byte select 3
U26	MByte_1	Memory byte select 1
V1	SBClk	Serial bus clock
V2	SPARE	
V3	VSAClk	VideoStream A clock
V4	VSAResetN	Video Stream reset
V5	GND	
V22	GND	
V23	MBank_0	Memory bank select 0
V24	MBank_1	Memory bank select 1
V25	MByte_2	Memory byte select 2
V26	MemClkRet_0	Memory Clock Return 0
W1	PLLPower	PLL Power/Gnd pin
W2	VSAData_5	VideoStream A data line 5
W3	VSAData_7	VideoStream A data line 7
W4	SBData	serial bus data
W5	VCC_3.3	
W22	VCC_3.3	
W23	MDSF	Memory DSF line
W24	MRAS	Memory RAS line
W25	MCAS	Memory CAS line
W26	MClkE	Memory clock enable
Y1	VSAData_3	VideoStream A data line 3
Y2	VSAData_6	VideoStream A data line 6
Y3	VSAData_4	VideoStream A data line 4
Y4	PLLGND	PLL Power/Gnd pin

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
Y5	VCC_3.3	
Y22	VCC_3.3	
Y23	MAddr_9	Memory address line 9
Y24	MAddr_10	Memory address line 10
Y25	MAddr_11	Memory address line 11
Y26	MWE	Memory write enable
AA1	RESERVED	No Connect
AA2	VSAdata_2	VideoStream A data line 2
AA3	VSAData_1	VideoStream A data line 1
AA4	VSAData_0	VideoStream A data line 0
AA5	GND	
AA22	GND	
AA23	MAddr_5	Memory address line 5
AA24	MAddr_6	Memory address line 6
AA25	MAddr_7	Memory address line 7
AA26	MAddr_8	Memory address line 8
AB1	PCIFIFOInDis	Delta control
AB2	PCIFIFOOutDis	Delta control
AB3	PCIRSTN	PCI reset
AB4	RESERVED	No Connect
AB5	GND	
AB6	GND	
AB7	VCC_3.3	
AB8	VCC_3.3	
AB9	GND	
AB10	GND	
AB11	VCC_3.3	
AB12	VCC_3.3	
AB13	GND	
AB14	GND	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
AB15	VCC_3.3	
AB16	VCC_3.3	
AB17	GND	
AB18	GND	
AB19	VCC_3.3	
AB20	VCC_3.3	
AB21	GND	
AB22	GND	
AB23	MemClkOut_0	Memory Clock Out 0
AB24	MAddr_2	Memory address line 2
AB25	MAddr_3	Memory address line 3
AB26	MAddr_4	Memory address line 4
AC1	PCIClkSel	33/66 MHz PCI Select
AC2	PCICLK	PCI clock
AC3	VDDQ_5	
AC4	VCC_2.5	
AC5	AGPSt_2	AGP status 2
AC6	AGPSBA_0	AGP Sideband Address 0
AC7	AGPSBA_3	AGP Sideband Address 3
AC8	AGPSBA_4	AGP Sideband Address 4
AC9	VDDQ_6	
AC10	PCIAD_29	PCI address/data line 29
AC11	PCIAD_26	PCI address/data line 26
AC12	PCIAD_23	PCI address/data line 23
AC13	PCIAD_21	PCI address/data line 21
AC14	PCIAD_20	PCI address/data line 20
AC15	PCICBEN_2	PCI byte enable 2
AC16	PCIFrameN	PCI frame signal
AC17	VDDQ_7	
AC18	PCIAD_15	PCI address/data line 15

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
AC19	PCIAD_12	PCI address/data line 12
AC20	PCIAD_8	PCI address/data line 8
AC21	AGPADSTB0N	AGP AD 2X strobe
AC22	PCIAD_4	PCI address/data line 4
AC23	VCC_2.5	
AC24	MemClkOut_1	Memory clock out 1
AC25	MAddr_0	Memory address line 0
AC26	MAddr_1	Memory address line 1
AD1	PCIIntAN	PCI interrupt
AD2	GND_0	
AD3	VCC_2.5	
AD4	AGPSt_0	AGP status 0
AD5	AGPRbfN	AGP Read Data Buffer full
AD6	GND_1	
AD7	AGPSBSTB	AGP Sideband Address 2X strobe
AD8	AGPSBA_5	AGP Sideband Address 5
AD9	AGPSBA_7	AGP Sideband Address 7
AD10	GND_2	
AD11	PCIAD_25	PCI address/data line 25
AD12	PCIAD_24	PCI address/data line 24
AD13	PCIAD_22	PCI address/data line 22
AD14	VDDQ_3	
AD15	PCIAD_16	PCI address/data line 16
AD16	PCIDevSelN	PCI device select
AD17	PCIStopN	PCI stop
AD18	GND_4	
AD19	PCIAD_11	PCI address/data line 11
AD20	PCICBEN_0	PCI byte enable 0
AD21	PCIAD_7	PCI address/data line 7
AD22	VDDQ_8	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
AD23	AGPvREF	not connected
AD24	VCC_2.5	
AD25	MemClkOut_2	Memory Clock Out 2
AD26	MemClkOut_3	Memory Clock Out 3
AE1	VCC_2.5	
AE2	VCC_2.5	
AE3	PCIReqN	PCI request
AE4	AGPSt_1	AGP status 1
AE5	AGPPipeN	AGP Pipelined Address
AE6	AGPSBA_1	AGP Sideband Address 1
AE7	AGPSBSTEN	
AE8	AGPSBA_6	AGP Sideband Address 6
AE9	PCIAD_31	PCI address/data line 31
AE10	PCIAD_28	PCI address/data line 28
AE11	AGPADSTB1N	
AE12	PCICBEN_3	PCI byte enable 3
AE13	PCIAD_19	PCI address/data line 19
AE14	PCIAD_17	PCI address/data line 17
AE15	PCIIRdyN	PCI parity
AE16	PCITRdyN	PCI T ready
AE17	PCIPar	PCI ready
AE18	PCIAD_14	PCI address/data line 14
AE19	PCIAD_10	PCI address/data line 10
AE20	AGPADSTB0	AGP AD 2X strobe
AE21	PCIAD_6	PCI address/data line 6
AE22	PCIAD_3	PCI address/data line 3
AE23	PCIAD_1	PCI address/data line 1
AE24	RESERVED	
AE25	VCC_2.5	
AE26	VCC_2.5	

Table 8-1   Pinlist by Number

NO.	NAME	DESCRIPTION
AF1	VCC_2.5	
AF2	VCC_2.5	
AF3	PCIGntN	PCI grant signal
AF4	VDDQ_0	
AF5	WbfN	
AF6	AGPSBA_2	AGP Sideband Address 2
AF7	PINAGPTol0	
AF8	VDDQ_1	
AF9	PCIAD_30	PCI address/data line 30
AF10	PCIAD_27	PCI address/data line 27
AF11	AGPADSTB1	AGP AD 2X strobe
AF12	VDDQ_2	
AF13	PCIIdSel	PCI ID select
AF14	PCIAD_18	PCI address/data line 18
AF15	AGPtol1	V tolerant AGP I/Os
AF16	GND_3	
AF17	PCICBEN_1	PCI byte enable 1
AF18	PCIAD_13	PCI address/data line 13
AF19	PCIAD_9	PCI address/data line 9
AF20	VDDQ_4	
AF21	PCIAD_5	PCI address/data line 5
AF22	PCIAD_2	PCI address/data line 2
AF23	PCIAD_0	PCI address/data line 0
AF24	GND_5	
AF25	VCC_2.5	
AF26	VCC_2.5	

8.2   Pinlist by Name

The table below provides a brief description of each pin. It is organized alphabetically by pin name.

The pin type definitions used are:

*   I/O: Input Signal

*   GND: Ground

*   VSS_3.3: Power at 3.3V

*   VSS_2.5: Power at 2.5 Volts

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
AGPADSTB0	AE20	AGP AD 2X strobe
AGPADSTB1	AF11	AGP AD 2X strobe
AGPADSTB0N	AC21	AGP AD 2x strobe
AGPADSTB1N	AE11	
AGPPipeN	AE5	AGP Pipelined address
AGPRbfN	AD5	AGP Read Data Buffer full
AGPSBA_0	AC6	AGP Sideband Address 0
AGPSBA_1	AE6	AGP Sideband Address 1
AGPSBA_2	AF6	AGP Sideband Address 2
AGPSBA_3	AC7	AGP Sideband Address 3
AGPSBA_4	AC8	AGP Sideband Address 4
AGPSBA_5	AD8	AGP Sideband Address 5
AGPSBA_6	AE8	AGP Sideband Address 6
AGPSBA_7	AD9	AGP Sideband Address 7
AGPSBSTB	AD7	AGP Sideband Address 2X strobe
AGPSBSTEN	AE7	
AGPSt_0	AD4	AGP status 0
AGPSt_1	AE4	AGP status 1
AGPSt_2	AC5	AGP status 2
AGPtol1	AF15	V tolerant AGP I/Os
AGPvREF	AD23	no connection
DacAGnd	R4	DAC Power/Gnd pin
DacAVDD	N1	Analog Video DAC
DacComp	P2	Compensation pin
GND	E5	
GND	E6	
GND	E9	
GND	E10	
GND	E13	
GND	E14	
GND	E17	
GND	E18	
GND	E21	
GND	E22	
GND	F5	

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
GND	F22	
GND	J5	
GND	J22	
GND	K5	
GND	K22	
GND	L11	
GND	L12	
GND	L13	
GND	L14	
GND	L15	
GND	L16	
GND	M11	
GND	M12	
GND	M13	
GND	M14	
GND	M15	
GND	M16	
GND	N5	
GND	N11	
GND	N12	
GND	N13	
GND	N14	
GND	N15	
GND	N16	
GND	N22	
GND	P5	
GND	P11	
GND	P12	
GND	P13	
GND	P14	
GND	P15	
GND	P16	
GND	P22	
GND	R11	
GND	R12	
GND	R13	
GND	R14	
GND	R15	
GND	R16	
GND	T11	
GND	T12	
GND	T13	
GND	T14	
GND	T15	
GND	T16	
GND	U5	
GND	U22	
GND	V5	
GND	V22	
GND	AA5	
GND	AA22	
GND	AB5	

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
GND	AB6	
GND	AB9	
GND	AB10	
GND	AB13	
GND	AB14	
GND	AB17	
GND	AB18	
GND	AB21	
GND	AB22	
GND_0	AD2	
GND_1	AD6	
GND_2	AD10	
GND_3	AF16	
GND_4	AD18	
GND_5	AF24	
MAddr_0	AC25	Memory address line 0
MAddr_1	AC26	Memory address line 1
MAddr_2	AB24	Memory address line 2
MAddr_3	AB25	Memory address line 3
MAddr_4	AB26	Memory address line 4
MAddr_5	AA23	Memory address line 5
MAddr_6	AA24	Memory address line 6
MAddr_7	AA25	Memory address line 7
MAddr_8	AA26	Memory address line 8
MAddr_9	Y23	Memory address line 9
MAddr_10	Y24	Memory address line 10
MAddr_11	Y25	Memory address line 11
MBank_0	V23	Memory bank select 0
MBank_1	V24	Memory bank select 1
MBank_2	U23	Memory bank select 2
MBank_3	J26	Memory bank select 3
MByte_0	U24	Memory byte select 0
MByte_1	U26	Memory byte select 1
MByte_2	V25	Memory byte select 2
MByte_3	U25	Memory byte select 3
MByte_4	G23	Memory byte select 4
MByte_5	H25	Memory byte select 5
MByte_6	H24	Memory byte select 6
MByte_7	G24	Memory byte select 7
MByte_8	C18	Memory byte select 8
MByte_9	B19	Memory byte select 9
MByte_10	C19	Memory byte select 10
MByte_11	B18	Memory byte select 11
MByte_12	D8	Memory byte select 12
MByte_13	C9	Memory byte select 13
MByte_14	D9	Memory byte select 14
MByte_15	B9	Memory byte select 15
MCAS	W25	Memory CAS line
MClkE	W26	Memory clock enable
MDat_0	L24	Memory data line 0
MDat_1	L25	Memory data line 1
MDat_2	L26	Memory data line 2

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
MDat_3	L23	Memory data line 3
MDat_4	M26	Memory data line 4
MDat_5	M25	Memory data line 5
MDat_6	M24	Memory data line 6
MDat_7	M23	Memory data line 7
MDat_8	T24	Memory data line 8
MDat_9	T25	Memory data line 9
MDat_10	T26	Memory data line 10
MDat_11	T23	Memory data line 11
MDat_12	R26	Memory data line 12
MDat_13	R25	Memory data line 13
MDat_14	R24	Memory data line 14
MDat_15	R23	Memory data line 15
MDat_16	N23	Memory data line 16
MDat_17	N26	Memory data line 17
MDat_18	N25	Memory data line 18
MDat_19	N24	Memory data line 19
MDat_20	P23	Memory data line 20
MDat_21	P26	Memory data line 21
MDat_22	P25	Memory data line 22
MDat_23	P24	Memory data line 23
MDat_24	K23	Memory data line 24
MDat_25	K24	Memory data line 25
MDat_26	K25	Memory data line 26
MDat_27	K26	Memory data line 27
MDat_28	J25	Memory data line 28
MDat_29	J24	Memory data line 29
MDat_30	J23	Memory data line 30
MDat_31	H23	Memory data line 31
MDat_32	D21	Memory data line 32
MDat_33	C22	Memory data line 33
MDat_34	B22	Memory data line 34
MDat_35	A22	Memory data line 35
MDat_36	A23	Memory data line 36
MDat_37	B23	Memory data line 37
MDat_38	A24	Memory data line 38
MDat_39	B24	Memory data line 39
MDat_40	G25	Memory data line 40
MDat_41	G26	Memory data line 41
MDat_42	F26	Memory data line 42
MDat_43	F25	Memory data line 43
MDat_44	F24	Memory data line 44
MDat_45	F23	Memory data line 45
MDat_46	E24	Memory data line 46
MDat_47	E23	Memory data line 47
MDat_48	C23	Memory data line 48
MDat_49	C25	Memory data line 49
MDat_50	C26	Memory data line 50
MDat_51	D24	Memory data line 51
MDat_52	D25	Memory data line 52
MDat_53	D26	Memory data line 53
MDat_54	E26	Memory data line 54

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
MDat_55	E25	Memory data line 55
MDat_56	D20	Memory data line 56
MDat_57	C21	Memory data line 57
MDat_58	B21	Memory data line 58
MDat_59	A21	Memory data line 59
MDat_60	A20	Memory data line 60
MDat_61	B20	Memory data line 61
MDat_62	C20	Memory data line 62
MDat_63	D19	Memory data line 63
MDat_64	D12	Memory data line 64
MDat_65	C12	Memory data line 65
MDat_66	B12	Memory data line 66
MDat_67	C13	Memory data line 67
MDat_68	D14	Memory data line 68
MDat_69	B13	Memory data line 69
MDat_70	A13	Memory data line 70
MDat_71	D13	Memory data line 71
MDat_72	D17	Memory data line 72
MDat_73	C17	Memory data line 73
MDat_74	B17	Memory data line 74
MDat_75	A18	Memory data line 75
MDat_76	A17	Memory data line 76
MDat_77	A16	Memory data line 77
MDat_78	B16	Memory data line 78
MDat_79	C16	Memory data line 79
MDat_80	C14	Memory data line 80
MDat_81	B14	Memory data line 81
MDat_82	A14	Memory data line 82
MDat_83	A15	Memory data line 83
MDat_84	D16	Memory data line 84
MDat_85	B15	Memory data line 85
MDat_86	C15	Memory data line 86
MDat_87	D15	Memory data line 87
MDat_88	C11	Memory data line 88
MDat_89	B11	Memory data line 89
MDat_90	A11	Memory data line 90
MDat_91	A12	Memory data line 91
MDat_92	D11	Memory data line 92
MDat_93	B10	Memory data line 93
MDat_94	C10	Memory data line 94
MDat_95	D10	Memory data line 95
MDat_96	C4	Memory data line 96
MDat_97	B4	Memory data line 97
MDat_98	A4	Memory data line 98
MDat_99	B3	Memory data line 99
MDat_100	D2	Memory data line 100
MDat_101	E2	Memory data line 101
MDat_102	E3	Memory data line 102
MDat_103	F3	Memory data line 103
MDat_104	A9	Memory data line 104
MDat_105	D7	Memory data line 105
MDat_106	C8	Memory data line 106

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
MDat_107	B8	Memory data line 107
MDat_108	B7	Memory data line 108
MDat_109	C7	Memory data line 109
MDat_110	D6	Memory data line 110
MDat_111	A8	Memory data line 111
MDat_112	A6	Memory data line 112
MDat_113	A5	Memory data line 113
MDat_114	C5	Memory data line 114
MDat_115	B5	Memory data line 115
MDat_116	B6	Memory data line 116
MDat_117	C6	Memory data line 117
MDat_118	D5	Memory data line 118
MDat_119	A7	Memory data line 119
MDat_120	F1	Memory data line 120
MDat_121	E1	Memory data line 121
MDat_122	D1	Memory data line 122
MDat_123	C1	Memory data line 123
MDat_124	A3	Memory data line 124
MDat_125	C2	Memory data line 125
MDat_126	D3	Memory data line 126
MDat_127	E4	Memory data line 127
MDSF	W23	Memory DSF line
MemClkOut_0	AB23	Memory Clock Out 0
MemClkOut_1	AC24	Memory Clock Out 1
MemClkOut_2	AD25	Memory Clock Out 2
MemClkOut_3	AD26	Memory Clock Out 3
MemClkRet_0	V26	Memory Clock Return 0
MemClkRet_1	H26	Memory Clock Return 1
MemClkRet_2	A19	Memory Clock Return 2
MemClkRet_3	A10	Memory Clock Return 3
MRAS	W24	Memory RAS line
MWE	Y26	Memory write enable
PCIAD_0	AF23	PCI address/data line 0
PCIAD_1	AE23	PCI address/data line 1
PCIAD_10	AE19	PCI address/data line 10
PCIAD_11	AD19	PCI address/data line 11
PCIAD_12	AC19	PCI address/data line 12
PCIAD_13	AF18	PCI address/data line 13
PCIAD_14	AE18	PCI address/data line 14
PCIAD_15	AC18	PCI address/data line 15
PCIAD_16	AD15	PCI address/data line 16
PCIAD_17	AE14	PCI address/data line 17
PCIAD_18	AF14	PCI address/data line 18
PCIAD_19	AE13	PCI address/data line 19
PCIAD_2	AF22	PCI address/data line 2
PCIAD_20	AC14	PCI address/data line 20
PCIAD_21	AC13	PCI address/data line 21
PCIAD_22	AD13	PCI address/data line 22
PCIAD_23	AC12	PCI address/data line 23
PCIAD_24	AD12	PCI address/data line 24
PCIAD_25	AD11	PCI address/data line 25
PCIAD_26	AC11	PCI address/data line 26

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
PCIAD_27	AF10	PCI address/data line 27
PCIAD_28	AE10	PCI address/data line 28
PCIAD_29	AC10	PCI address/data line 29
PCIAD_3	AE22	PCI address/data line 3
PCIAD_30	AF9	PCI address/data line 30
PCIAD_31	AE9	PCI address/data line 31
PCIAD_4	AC22	PCI address/data line 4
PCIAD_5	AF21	PCI address/data line 5
PCIAD_6	AE21	PCI address/data line 6
PCIAD_7	AD21	PCI address/data line 7
PCIAD_8	AC20	PCI address/data line 8
PCIAD_9	AF19	PCI address/data line 9
PCICBEN_0	AD20	PCI byte enable 0
PCICBEN_1	AF17	PCI byte enable 1
PCICBEN_2	AC15	PCI byte enable 2
PCICBEN_3	AE12	PCI byte enable 3
PCICLK	AC2	PCI clock
PCIClkSel	AC1	33/66 MHz PCI select
PCIDevSelN	AD16	PCI device select
PCIFIFOInDis	AB1	Delta control
PCIFIFOOutDis	AB2	Delta control
PCIFrameN	AC16	PCI frame signal
PCIGntN	AF3	PCI grant signal
PCIIdSel	AF13	PCI ID select
PCIIntAN	AD1	PCI interrupt
PCIIRdyN	AE15	PCI parity
PCIPar	AE17	PCI ready
PCIReqN	AE3	PCI request
PCIRSTN	AB3	PCI reset
PCIStopN	AD17	PCI stop
PCITRdyN	AE16	PCI T ready
PINAGPTol0	AF7	
PLLDISABLE	T3	PLL Disable
PLLPower	W1	PLL Power/Gnd pin
PLLGND	Y4	PLL Power/Gnd pin
RenderSyncN	D18	Multirasterizer i/o sync pin
RESERVED	AE24	
RESERVED	AA1	No Connect
RESERVED	AB4	No Connect
ROMSelN	U2	ROM select signal
ROMWeN	U1	ROM write wnable
SBClk	V1	serial bus clock
SBData	W4	serial bus data
SPARE	V2	
SPARE	J4	
TestMode	R1	Test Mode control
TestSel_0_	M1	Test Mode select 0
TestSel_1	R3	Test Mode select
TestSel_2_	M2	Test Mode select 1
VCC_2.5	D4	
VCC_2.5	A1	
VCC_2.5	B1	

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
VCC_2.5	AE1	
VCC_2.5	AE2	
VCC_2.5	AD3	
VCC_2.5	AC4	
VCC_2.5	AF1	
VCC_2.5	AF2	
VCC_2.5	AF25	
VCC_2.5	AE25	
VCC_2.5	AD24	
VCC_2.5	AC23	
VCC_2.5	AF26	
VCC_2.5	AE26	
VCC_2.5	B26	
VCC_2.5	B25	
VCC_2.5	C24	
VCC_2.5	D23	
VCC_2.5	A26	
VCC_2.5	A25	
VCC_2.5	B2	
VCC_2.5	A2	
VCC_2.5	C3	
VCC_3.3	E7	
VCC_3.3	E8	
VCC_3.3	E11	
VCC_3.3	E12	
VCC_3.3	E15	
VCC_3.3	E16	
VCC_3.3	E19	
VCC_3.3	E20	
VCC_3.3	G5	
VCC_3.3	G22	
VCC_3.3	H5	
VCC_3.3	H22	
VCC_3.3	L5	
VCC_3.3	L22	
VCC_3.3	M5	
VCC_3.3	M22	
VCC_3.3	R5	
VCC_3.3	R22	
VCC_3.3	T5	
VCC_3.3	T22	
VCC_3.3	W5	
VCC_3.3	W22	
VCC_3.3	Y5	
VCC_3.3	Y22	
VCC_3.3	AB7	
VCC_3.3	AB8	
VCC_3.3	AB11	
VCC_3.3	AB12	
VCC_3.3	AB15	
VCC_3.3	AB16	
VCC_3.3	AB19	

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
VCC_3.3	AB20	
VDDQ_0	AF4	
VDDQ_1	AF8	
VDDQ_2	AF12	
VDDQ_3	AD14	
VDDQ_4	AF20	
VDDQ_5	AC3	
VDDQ_6	AC9	
VDDQ_7	AC17	
VDDQ_8	AD22	
vidBlue	P3	Analog blue signal
VidDDCClk	U4	Clock line for DDC
VidDDCData	U3	Data line for DDC
VideoExtCtrl	D22	Video external control
vidGreen	N3	Analog green signal
VidHSync	R2	Horizontal sync
vidRed	N2	Analog red signal
vidResRef	P4	Reference resistor
VidRightEye	N4	Right signal for stereo
VidVRef	P1	Voltage reference
VidVsync	T2	Vertical sync
VSAClk	V3	VideoStream A clock
VSAData_0	AA4	VideoStream A data line 0
VSAData_1	AA3	VideoStream A data line 1
VSAdata_2	AA2	VideoStream A data line 2
VSAData_3	Y1	VideoStream A data line 3
VSAData_4	Y3	VideoStream A data line 4
VSAData_5	W2	VideoStream A data line 5
VSAData_6	Y2	VideoStream A data line 6
VSAData_7	W3	VideoStream A data line 7
VSAResetN	V4	Video Stream reset
VSBClk	H4	VideoStream B clock
VSBClkOut	J3	Video Stream B clock out
VSBData_0	F4	VideoStream B data line 0
VSBData_1	G1	VideoStream B data line 1
VSBData_2	G2	VideoStream B data line 2
VSBData_3	G3	VideoStream B data line 3
VSBData_4	G4	VideoStream B data line 4
VSBData_5	H1	VideoStream B data line 5
VSBData_6	H2	VideoStream B data line 6
VSBData_7	H3	VideoStream B data line 7
VSBResetN	F2	Video Stream B Reset Out
VSCtl_0	K1	VideoStreams Control line 0
VSCtl_1	K2	VideoStreams Control line 1
VSCtl_2	L4	VideoStreams Control line 2
VSCtl_3	L1	VideoStreams Control line 3
VSCtl_4	L2	VideoStreams Control line 4
VSCtl_5	L3	VideoStreams Control line 5
VSCtl_6	M3	VideoStreams Control line 6
VSCtl_7	M4	VideoStreams Control line 7
VSGPChipSelectN	K3	VS GP bus chip select
VSGPDataAckN	K4	VS GP bus data ack

Table 8-2   Pinlist by Name

NAME	NO.	DESCRIPTION
VSGPDataStrob eN	J1	VS GP bus data strobe
VSGPReadWrit eN	J2	VS GP bus read/write signal
WbfN	AF5	
Xtal1	T1	Crystal i/p 1
Xtal2	T4	Crystal i/p 2