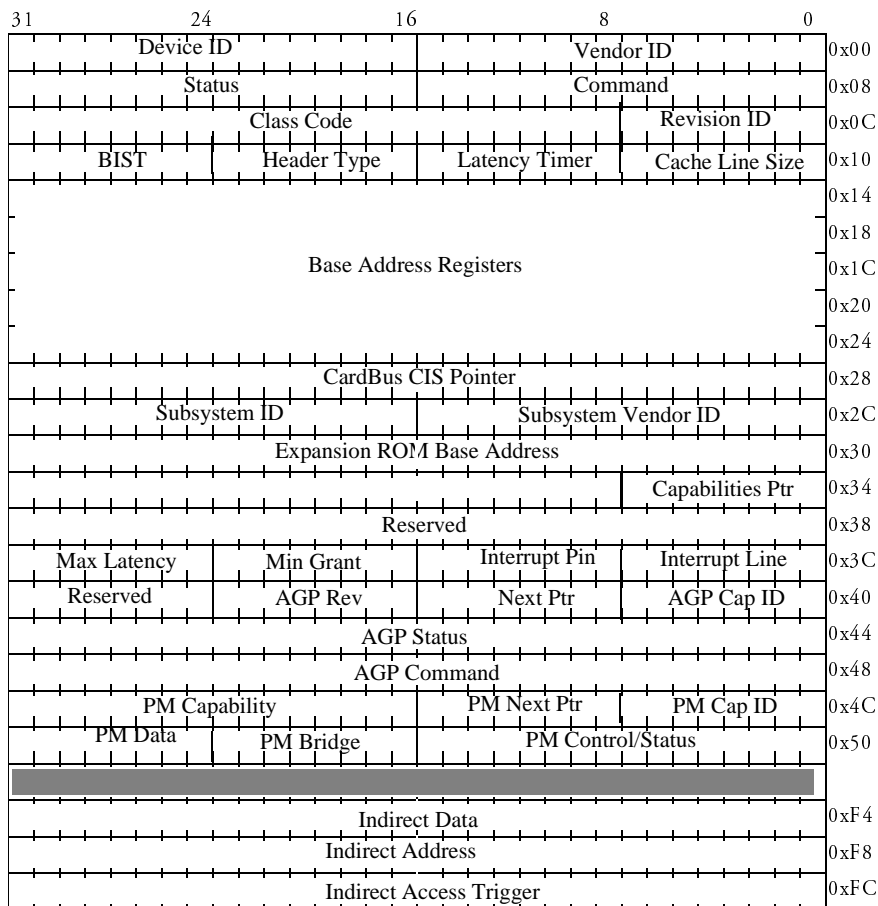# 2

Address Maps and Regions

2.1   PCI Configuration Region

The PCI Configuration Region provides information that satisfies the needs of current and anticipated system configuration mechanisms.

Figure 2-1 PCI Configuration Region

31	24	16	8	0	
Device ID		Vendor ID			0x00
Status		Command			0x08
Class Code			Revision ID		0x0C
BIST	Header Type	Latency Timer	Cache Line Size		0x10
					0x14
					0x18
Base Address Registers					0x1C
					0x20
					0x24
CardBus CIS Pointer					0x28
Subsystem ID		Subsystem Vendor ID			0x2C
Expansion ROM Base Address					0x30
			Capabilities Ptr		0x34
Reserved					0x38
Max Latency	Min Grant	Interrupt Pin	Interrupt Line		0x3C
Reserved	AGP Rev	Next Ptr	AGP Cap ID		0x40
AGP Status					0x44
AGP Command					0x48
PM Capability		PM Next Ptr	PM Cap ID		0x4C
PM Data	PM Bridge	PM Control/Status			0x50
Indirect Data					0xF4
Indirect Address					0xF8
Indirect Access Trigger					0xFC

2.2   Region Zero Address Map

The P~ERMEDIA~ 3 region zero address map is shown in Table 2-1.

Table 2-1   Region Zero Address Map

Address Range	Region Select	Byte Swap/ Write Combined
0000.0000 -> 0000.02FF	Control Status	No
0000.0300 -> 0000.03FF	Bypass Control	No
0000.0400 -> 0000.0FFF	Repeat of the Control and Bypass Decodes	No
0000.1000 -> 0000.1FFF	Memory Control	No
0000.2000 -> 0000.2FFF	GP FIFO Access	No
0000.3000 -> 0000.30FF	Video Control	No
0000.3100 -> 0000.3FFF	Video Overlay Control	No
0000.4000 -> 0000.4FFF	RAMDAC	No
0000.5000 -> 0000.57FF	VS GP	No
0000.5800 -> 0000.5FFF	VSCtl	No
0000.6000 -> 0000.6FFF	VGA Control	No
0000.7000 -> 0000.7FFF	TextureData FIFO	No
0000.8000 -> 0000.FFFF	GP Registers	No
0001.0000 -> 0001.01FF	Control Status	Yes
0001.0300 -> 0001.03FF	Bypass Control	Yes
0001.0400 -> 0001.0FFF	Repeat of the Control and Bypass Decodes	Yes
0001.1000 -> 0001.1FFF	Memory Control	Yes
0001.2000 -> 0001.2FFF	GP FIFO Access	Yes
0001.3000 -> 0001.37FF	Video Control	Yes
0001.3800 -> 0001.3FFF	Video Overlay Control	Yes
0001.4000 -> 0001.4FFF	RAMDAC	Yes
0001.5000 -> 0001.57FF	VS GP	Yes
0001.5800 -> 0001.5FFF	VSCtl	Yes
0001.6000 -> 0001.6FFF	VGA Control	Yes
0001.7000 -> 0001.7FFF	TextureData FIFO	Yes
0001.8000 -> 0001.FFFF	GP Registers	Yes

2.3   PCI Address Regions

PERMEDIA 3 has seven base address regions, as shown in Table 2-2.

Table 2-2   PERMEDIA 3 PCI Address Regions

Region	Address Space	Bytes	Description	Comments
Config	Configuration	256	PCI Configuration	PCI special
Zero	Memory	128 K	Control Registers	Relocatable
One	Memory	64M	Memory Aperture One	Relocatable
Two	Memory	64M	Memory Aperture Two	Relocatable
Three	I/O	16	Indirect Access I/O	Optional and Relocatable
ROM	Memory	64 K	Expansion ROM	Relocatable
VGA	Memory & I/O	—	VGA Access	Optional and Fixed